Measurement of Thermoelectric Properties of Amorphous Silicon Based Thin Films

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MEASUREMENT OF THERMOELECTRIC PROPERTIES OF AMORPHOUS SILICON
BASED THIN FILMS

A DISSERTATION
PRESENTED TO THE FACULTY
OF NATURAL SCIENCES AND MATHEMATICS
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BY
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ADVISOR: PROFESSOR BARRY L. ZINK
Abstract

It is important to understand thermal transport behavior in materials for technological and fundamental physics applications. Many efforts have been made in the past for explaining thermal conduction in solids. It has been observed that thermal transport properties may change with reducing size of the sample, especially as sample size approaches the nanoscale regime. The deviation in these properties, mainly in thermal conductivity, may change the choice of the material for different applications such as thermoelectricity. Thermoelectric materials are a possible source of sustainable energy and can play an important role in the fight against the present energy crisis. Recently, better thermoelectric materials have become available in bulk form as compared to thin film form, with higher figure of merit ($ZT = \alpha^2 \sigma T/k$). $ZT$ is a dimensionless quantity which is used to characterize the performance of thermoelectric materials in terms of the efficiency. Figure of merit ($ZT$) depends on three fundamental properties including thermal conductivity ($k$) which is challenging to measure for thin films. This is due to several reasons such as large or more than one background contribution and radiation heating above 100 K. Precise measurements of thermopower ($\alpha$) also become critical for thin films in order to calculate $ZT$ and the efficiency. For devices which rely on thin film technology it is important to have an accurate knowledge of how a material behaves as a thin film in a wide range of temperature. All three of these properties are a function of charge carrier concentration as well as of temperature. In my thesis, I will present novel experimental techniques and measurements of thermoelectric proper-
ties in amorphous based thin films over a wide range of temperature. Amorphous Si alloys are expected to have high efficiency for thermoelectric purposes because of their low thermal conductivity and the fact that we can control the charge carrier concentration for optimized thermopower($\alpha$) and electrical conductivity($\sigma$) by controlling the dopant concentration. Thermal properties of pure amorphous thin films are also potentially useful in micro- or nano fabrication techniques such as electrically insulating integrated devices.
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‘Gratitude is the memory of the heart.’

By Jean Baptiste Massieu

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Chapter 1

Introduction

This chapter gives an overall brief introduction of the contents of this dissertation. The goal of this document is to provide information about the thermal and thermoelectric transport in thin films and our research which was carried out to investigate potentially better thermoelectric thin films. A thermoelectric material converts heat energy into electrical energy. The main focus is on characterizing thermoelectric transport in amorphous silicon based thin films in the temperature range of 77 - 325 K. In the beginning chapters of this dissertation, several types of bulk and low dimensional thermoelectric materials are briefly discussed. The potential applications of these materials as a possible sustainable energy source, in refrigeration, and in heating will be addressed. The probable extension of these applications in micro- and nanotechnology gives motivation to characterize thermoelectric properties in thin films and nanostructures. When a material is grown as thin film, its physical properties often deviate from the bulk behavior. This presents a need to measure these properties, especially thermal conductivity, in thin films by developing effective measurement techniques. Thermal conductivity is a challenging property to measure in thin films due to several reasons which will be highlighted in this dissertation.
In the later chapters, a detailed description of our effective measurement technique to characterize the thermal and thermoelectric transport in thin film is provided. The heart of our technique is our micromachined silicon nitride based thermal isolation platform. The effectiveness of our technique is stated and proved by presenting measured data on thin films. A whole chapter is dedicated to further challenges which we face while measuring thermal conductivity of amorphous silicon based thin films. The effect of boundary scattering on thermal conductivity measurements in silicon nitride will also be discussed.

The performance of a thermoelectric material is defined by its three fundamental properties: thermal conductivity, thermopower and electrical conductivity. We studied these properties in two amorphous silicon metal alloy systems (Si-Cu and Si-Al) in thin film form. The measurement of these properties, results, and the potential of a-Si based thin film as thermoelectric films will be discussed. In the end, the technique of electron beam lithography which is required to scale down the platform to measure even smaller nanostructures, is described in detail. A few new methods of patterning nanostructures on suspended thermal isolation platforms will also be discussed. The overall goal is to investigate thin films and nanostructures for possibly better thermoelectric performance.
Chapter 2

Thermoelectrics

2.1 Introduction

This chapter provides an introduction to thermoelectric materials, the physics which dominates these materials, and potential applications in which they can be beneficial. Thermoelectric materials are capable of converting heat into electricity. This emerging class of materials has already been successfully used in the applications of power generation and thermoelectric refrigeration. Thermoelectric materials have recently gained more attention from researchers and scientists because they are expected to help combat global warming by contributing to present renewable energy sources. Diminishing energy reserves have created an urgent need for alternative energy sources such as thermoelectric materials. Scientists are investigating ways to optimize the efficiency in these materials for their potential contribution to sustainable energy sources. Similar applications can be implemented in micro and nanotechnology by using efficient thermoelectric thin films and nanostructures. Later sections of this chapter will provide information about recent discoveries of thermoelectric thin films and nanostructures. The fundamental properties on which the efficiency of a thermoelectric material depends and possible ideas to maximize this
efficiency will also be discussed.

2.2 Thermoelectric Effect

2.2.1 Seebeck Effect & Peltier Effect

The generation of a voltage across a thermoelectric material as a result of the temperature difference is known as the thermoelectric effect or more specifically the Seebeck Effect. Mathematically, it is expressed as,

$$\alpha = \frac{\Delta V}{\Delta T} \quad (2.2.1)$$

where $\alpha$ is the Seebeck coefficient (commonly known as thermopower) and $\Delta V$ is the voltage generated because of the temperature difference $\Delta T$ (see Figure 2.1). A greater value of $\alpha$ in a material implies that it converts heat into electrical energy efficiently, but there are other factors involved for a complete definition of the efficiency of thermoelectric materials which will be discussed later in this chapter.

On the other hand, if the situation is reversed by applying a current across a thermoelectric material, a temperature difference is produced. This is known as the Peltier effect[1]. Mathematically, it is expressed as,

$$\pi = \frac{q}{I} \quad (2.2.2)$$

where $\pi$ is the Peltier coefficient, $I$ is the applied current and $q$ is the rate of heating and cooling at both ends. The greater the temperature difference, the better could be the performance in heating or cooling application.
2.3 Thermoelectric Efficiency

In this section, the main focus is on describing the efficiency of a thermoelectric refrigerator (or generator) and the parameters which are important to define it. A thermoelectric material is essentially an energy conversion system and like any other energy conversion system, it obeys the laws of thermodynamics. Its performance is characterized in terms of its efficiency. Generally, the efficiency, $\eta$, of an energy conversion system is defined as a ratio of useful output (which can be used to perform work) to a given input. Mathematically, it is expressed as,

$$\eta = \frac{Output}{Input}$$  \hspace{1cm} (2.3.1)

In order to derive the efficiency of a thermoelectric system, we consider a simple example of a typical thermoelectric refrigerator which is shown in Fig.2.2a. It consists of a positive (p) and negative (n) branch attached with metal contacts. The p and n branches are p and n type semiconductors which is a semiconductor doped with materials which accepts and donates an electron respectively. In Figure 2.2 one end of these branches is attached with metal contacts to a heat source and other to the heat sink. The heat transported at these two junctions can be written
as a combination of heat transport due the Peltier effect and the heat conduction through the material. So we can write the heat transported through the p and n branches respectively as,

$$Q_p = \alpha_p IT - k_p A_p (dT/dx)$$ \hspace{1cm} (2.3.2)

$$Q_n = -\alpha_n IT - k_n A_n (dT/dx)$$ \hspace{1cm} (2.3.3)

where A, k, \(\alpha\) are the area, thermal conductivity and Seebeck coefficient of the two branches respectively and subscripts p and n relates to each branch. In these equations we must include the contribution from Joule heating per unit length (L) in each branch which is \(Q/L=I^2\rho/A\), where \(\rho\) is the resistivity and A is the area of each branch. Due to the Joule heating the temperature is not uniform across the length of p and n branches. This can be considered by taking a second order derivative of temperature gradient in the second term on right hand side of equations 2.3.2 and

Figure 2.2: (left) Thermoelectric Generator and (right) Thermoelectric Refrigerator.
2.3.3. For each branch this can expressed as,

\[-k_p \frac{d^2 T}{dx^2} = \frac{I^2 \rho_p}{A_p}\]  

(2.3.4)

\[-k_n \frac{d^2 T}{dx^2} = \frac{I^2 \rho_n}{A_n}\]  

(2.3.5)

These equations can further be solved for the rate of heat transport in each branch by using proper boundary conditions[2]. Then adding the two solutions give the cooling \((Q_c)\) that occurs at the hot junction.

\[Q_c = IT_1(\alpha_p - \alpha_n) - \left( \frac{I^2 R}{2} \right) - (T_2 - T_1)K\]  

(2.3.6)

In the application as a heat pump, the physics remains same but mathematical representation of heating power is slightly different. In heating application, the Joule heating term \(I^2 R/2\) in equation 2.3.6 becomes positive because it contributes to the overall heating effect. The heating power can be written as,

\[Q_h = IT_1(\alpha_p - \alpha_n) + \left( \frac{I^2 R}{2} \right) - (T_2 - T_1)K\]  

(2.3.7)

where \(T_1, T_2\) are the temperatures at cold and hot ends, \(R\) and \(K\) are total electrical resistance and total thermal conductance in two branches, and \(\alpha_p\) and \(\alpha_n\) are the Seebeck coefficients in two branches respectively. The Joule heating is divided equally between the hot and cold ends causing an increased heating at the hot end and a decreased cooling at the cold end. Therefore, the heating effect in enhanced as compared to cooling effect for similar materials used for heating and cooling applications, respectively.

The cooling power, \(Q_c\), is linearly dependent on current in the first term but on \(I^2\) in the second term (as shown in equation 2.3.6). Thus, there must be an optimum
value of current (I) for which $Q_c$ will have a maximum value. To find this value, we set $dQ_c/dI=0$ and get,

$$I = \frac{(\alpha_p - \alpha_n)T_1}{R} \quad (2.3.8)$$

After substituting equation 2.3.8 back in equation 2.3.6, we get the maximum cooling power as,

$$(Q_c)_{max} = \frac{T_1^2(\alpha_p - \alpha_n)^2}{2R} - (T_2 - T_1)K \quad (2.3.9)$$

Equation 2.3.9 also shows that if the temperature difference between the hot and cold end is large, maximum cooling can not be achieved. If we set $(Q_c)_{max}=0$, we can write the maximum temperature difference as,

$$(T_2 - T_1)_{max} = \frac{T_1^2(\alpha_p - \alpha_n)^2}{2KR} \quad (2.3.10)$$

where $\frac{(\alpha_p-\alpha_n)^2}{KR}=Z$, which is know as thermoelectric figure of merit and has units of K$^{-1}$. Sometimes it is defined as dimensionless when multiplied by the absolute temperature.

By now, we have a clear idea of what factors the maximum cooling power depends upon. Finally, we want to relate this maximum cooling power, $Q_c$, with efficiency or the performance of a thermoelectric refrigerator or heat pump. The thermoelectric efficiency is defined as,

$$\eta = \frac{\text{Maximum Cooling Power}}{\text{Rate at which electrical Energy is supplied}} \quad (2.3.11)$$

The electrical energy supplied to each p and n branch is given as [2],

$$W_p = I\alpha_p(T_2 - T_1) + \frac{I^2\rho_pL_p}{A_p} \quad (2.3.12)$$

$$W_n = I\alpha_n(T_2 - T_1) + \frac{I^2\rho_nL_n}{A_n} \quad (2.3.13)$$
Summing equations 2.3.12 & 2.3.13 gives total electrical power supplied (W),

\[ W = I(\alpha_p - \alpha_n)(T_2 - T_1) + I^2R \]  

(2.3.14)

Then using equations 2.3.9 & 2.3.14 in equation 2.3.11, we get,

\[ \eta = \frac{T_1^2(\alpha_p - \alpha_n)^2 - (T_2 - T_1)K}{I(\alpha_p - \alpha_n)(T_2 - T_1) + I^2R} \]  

(2.3.15)

To find the maximize value of this efficiency we find the maximum current by setting \( d\eta/dI = 0 \), which gives,

\[ (I\eta)_{max} = \frac{(\alpha_p - \alpha_n)(T_2 - T_1)}{R[(1 + ZT_{av})^{1/2} - 1]} \]  

(2.3.16)

Hence the efficiency becomes,

\[ \eta = \left( \frac{T_1}{T_2 - T_1} \right)^\frac{[(1 + ZT_{av})^{1/2} - \frac{T_2}{T_1}]}{[(1 + ZT_{av})^{1/2} + 1]} \]  

(2.3.17)

Where \( T_{av} = (T_2 + T_1)/2 \) is the average temperature between hot and cold ends and \( Z \) is the figure of merit.

### 2.4 Figure of Merit

It is clear from the discussion in previous section that in order to increase the performance of a thermoelectric material, we need to increase the dimensionless figure of merit, \( ZT \) (extracted from equation 2.3.10) which is generally written as,

\[ ZT = \frac{\alpha^2T}{KR} \]  

(2.4.1)
where \( \alpha \) is the thermopower, \( K \) and \( R \) are the thermal conductance and resistance of the material, and \( T \) is the absolute temperature. If we exclude the geometry contribution by using thermal conductivity \( (k) \) and electrical resistivity \( (\rho) \) (or electrical conductivity, \( \rho = 1/\sigma \)) instead of thermal conductance \( (K) \) and resistance \( (R) \), we can then rewrite \( ZT \) as,

\[
ZT = \frac{\alpha^2 \sigma T}{k}
\]

This implies that in order to optimize the performance of a thermoelectric material we optimize these three properties, \( k, \alpha, \sigma \), as a function of temperature. We can do this by investigating potential thermoelectric materials and developing efficient measurement technique to measure these properties. Later in this chapter, we discuss these properties in details for different types of materials. Though these properties are not assumed to be geometrically dependent, there is evidence that they are affected in low dimensional materials.

### 2.4.1 Thermal Conductivity

Thermal conductivity is an important intrinsic property of a material. Since \( k \) appears in dominator of the equation 2.4.2, it implies that reducing \( k \) is one way to increase \( ZT \). In different types of materials, thermal transport is governed by different processes[3]. For example, in metals, heat conduction is dominated by electrons. Metals have very good electrical conductivity (which is another way to increase \( ZT \)) but at the same time they are very good heat conductors and have relatively low thermopower. This makes metals a poor choice as a thermoelectric. On the other extreme, insulators are very bad heat conductors because heat transport is only through lattice vibrations (phonons) but insulators also do not conduct electrical current at all due to the lack of the electronic contribution. This makes them a bad candidate for thermoelectric applications.
Figure 2.3: Schematic dependence[1] of a)Seebeck coefficient \( (\alpha) \) and electrical conductivity \( (\sigma) \), optimize power factor \( (\alpha^2\sigma) \) for a specific concentration b)Lattice and electronic thermal conductivity \( (k) \) on charge carrier concentration.

However, another intermediate class of materials exists between insulators and metals called \textit{semiconductors} in which electrical properties can be controlled by doping or alloying.

\subsection{2.4.2 Thermopower and electrical conductivity}

The origin of thermopower generation is the diffusion of charge carriers due to the thermal agitation between the hot and cold end of the material. For materials that can be described using a single electronic band structure such as typical metals, diffusion thermopower \( (\alpha_d) \) is mathematically represented as,

\[
\alpha_d = \left( \frac{\pi^2 k_B^2 T}{3|e|} \right) \left| \frac{d\sigma(E)}{dE} \right|_{E=E_F}
\]

(2.4.3)

where \( k_B \) is the Boltzmann constant, \( e \) is the charge on an electron or hole and \( \sigma(E) \) is the electronic density of states near Fermi level \( E_F \). So the charge carrier density is an important aspect in defining thermopower and determining its sign. In semiconductors, if the charge carriers are electrons, the developed voltage is negative whereas it is positive for holes. However, for metals there is an additional term in
equation 2.4.3. The contribution of the second term is the slope of the Fermi surface which often decides the sign of the thermopower[4].

The electrical conductivity is also a the function of charge carrier concentration and band structure in a material. Figure 2.3 shows the variation of electronic thermal conductivity, thermopower and electrical conductivity for bulk isotropic materials as a function of charge carrier concentrations for insulators, semiconductors and metals. We see that lattice thermal conductivity is not affected by carrier concentration. Figure 2.3 shows that in semiconductors, an optimized value of the electrical power factor ($\sigma\alpha^2$) can be determined by varying the carrier concentration. These properties (thermal conductivity, thermopower and electrical conductivity) may deviate[5] from their bulk behavior with the reduction of sample size. In order to find a potentially better low dimensional thermoelectric material it is important to study these three properties individually by developing effective measurement techniques.

2.5 Present Thermoelectrics

Usually all conductors (e.g, Au, Cu, Pt etc) exhibit thermoelectric (TE) phenomena but a material is said to be thermoelectric if it’s figure of merit (ZT) $> 0.5$ [1]. Researchers have been struggling to increase this factor by investigating new materials. This section provides a brief introduction of different types and structural forms of materials which are being investigated as thermoelectrics.

2.5.1 Bulk

Bismuth-Telluride, Bismuth-Antimony, and Bismuth Selenium alloys

The most popular thermoelectric material in bulk which has been commercially used is bismuth telluride (Bi$_2$Te$_3$) and it alloys. These materials are efficient in the temperature range of 200-400 K which limits their use. The structure of Bi-Te is
layered and has anisotropic thermal and electronic transport properties. The layers of Te-Te are held together by Van der Waal forces and the rest of the atoms are held together by strong ionic-covalent bonds[6]. The lattice thermal conductivity in this system varies inversely with temperature and gives low thermal conductivity as temperature increases. The thermal conductivity at 300 K is $\sim 2$ W/m K[7]. When Bi is alloyed with selenium and antimony with telluride in a solid solution form, thermal conductivity reduces without affecting the charge mobility [8]. Since the power factor in these alloys of Bi remains the same as Bi-Te, this gives an additional preference to these materials for thermoelectric application. Bismuth antimony on the other hand is useful for low temperature application because adding of about 0.15 Sn to Bi atomic ratio creates a narrow band gap [9]. This is very small for use at higher temperature but gives a good power factor for low temperatures use. Adding Sn also decreases thermal conductivity which increases the figure of merit.

**Germanium-Silicon (Ge-Si) Alloys**

Another thermoelectric compound which has been used for thermoelectric application is the Ge-Si alloy. Ge and Si usually have very high room temperature thermal conductivities (63 and 113 W/m K) but when $\sim 30\%$ of Ge is added in Si, the room temperature thermal conductivity reduces to 10 W/m K [10]. The reduction in thermal conductivity is caused by the scattering of low frequency phonons by grain boundaries which reduces the mean free path of phonons but the charge carriers have a higher mean free path than phonons[11]. This reduction in thermal conductivity without greatly effecting the carrier mobility works in favor of Ge-Si alloys as thermoelectrics.
Figure 2.4: Top: Schematic illustration of a (a) empty (Co-Sn) and (b) filled skutterudites (Ce/La-Fe$_4$Sn$_{12}$)[12] b) Bottom: The structure of a regular body centered cubic crystal.

Skutterudites

Skutterudites are another class of materials which is studied as potential thermoelectrics. Skutterudites are formed by a combination of a metal (M) atom with pnicogen (X, which are elements in group V in periodic table such as Phosphorus (P), Arsenic (As), Antimony (Sb)). The general chemical formula of these materials can written as $MX_3$. There are two structural forms of skutterudites (i) unfilled (binary) skutterudites (ii) filled skutterudites. An example of the structure of empty (Co-Sn) and filled skutterudites (Ce/La-Fe$_4$Sn$_{12}$) is shown in Figure 2.4.

Unfilled skutterudites crystallize in a bcc (body centered cubic) structure with spaces at the 12 coordinated position. Each metal atom is octahedrally surrounded by pnicogen forming an octahedron [13, 14]. These materials have excellent electronic properties and somewhat better thermopower. Their room temperature thermal conductivity is of the $\sim 10$ W/m K which is too high to give a good figure of merit at room temperature. For filled skutterudites, a guest atom (G) or ion is introduced into the 12 coordinated sites. The general chemical formula can be
written as $G_yM_4X_{12}$, where $y$ is the fraction of the guest ions. These guest ions or 'rattlers' can cause the low frequency heat carrying phonon to be scattered strongly enough to significantly reduce the thermal conductivity as compared to unfilled skutterudites\cite{15}. This reduction in thermal conductivity gives $ZT > 1$ between the temperature range of 500 K and 1000 K\cite{16, 17, 18, 19, 20, 21, 22}.

**Clathrates**

Clathrates is another class of materials which exhibit a periodic structure of tetrahedrally bonded atoms (e.g silicon, sermanium or tin) in the form of a cage which encloses a relatively large metal atom. The most interesting property of these material which makes them potential for thermoelectric study is their 'glass like' thermal conductivity. Theoretical estimations suggest a $ZT$ of 1.7 at high temperatures\cite{23}. A recent summary of estimated and experimental data of $ZT$ for this class of material can be found\cite{24}.

**2.5.2 Thin films and nanostructures**

Thermoelectric thin films and nanostructures have the same application importance as the bulk thermoelectric materials but for integrated devices and the systems which do not generate a large amount of heat. As we have seen in section 2.3, temperature difference across the hot and cold end of a thermoelectric material is also important. The challenge is to optimize the power factor ($\alpha^2\sigma$) while minimizing thermal conductivity at the same time. Scientist are investigating thin film version of bulk thermoelectrics as well as exploring potential thin films and nanostructures as thermoelectric materials. The main motivation of the study of low dimensional materials is the reduction of thermal conductivity with reducing sample size and exploring how thermopower is affected by by size reduction. This section discusses some advances in potential thin film and nano structured thermoelectrics.
Thin film & Quantum Dot Super Lattice

A superlattice is formed using a unique method of growth called epitaxial growth\cite{25} which generates periodic layers of material. The idea is to take advantage of sharp features in the electron density of states\cite{26} to improve the electronic performance and to reduce the phonon thermal conductivity through interface scattering\cite{27} by growing these superlattices. The group V-VI and group IV-VI compounds are semiconductors and have useful structural properties which are being tested in thin film form for potential thermoelectric materials. P-type Bi$_2$Te$_3$-Sb$_2$Te$_3$ superlattice thin films are discovered to have a ZT of 3.5 around room temperature\cite{28} where as Pb-SnSeTe/PbTe, and PbTeSe/PbTe quantum dot superlattices (QDSL) have a ZT of 1.8 and 1.5, respectively\cite{29, 30}. There are many other superlattice systems which are studied as potential thermoelectrics, such as Si-Ge superlattices\cite{31, 32, 33}, Bi/Sb superlattices\cite{34}, and skutterudite-based superlattices\cite{35}. A large reduction in in-plane thermal conductivity has been observed in Si-Ge and Si-SiGe alloy superlattices as compared to their similar alloys in the cross plane direction\cite{31, 32}. However for an equivalent composition, the in-plane thermal conductivities are comparable between the two\cite{36}. The thermopower measurements for Bi-Sb and skutterudite superlattices require more conclusive data\cite{37, 38}.

**Silicon Nanowires**

It is a well known fact that silicon is a good thermal conductor at room temperature and thus it is a poor thermoelectric with figure of merit, \(ZT \sim 0.01\)\cite{39}. Recently discovered silicon nanowires\cite{5, 40} give a \(ZT \sim 0.6\) and \(ZT \sim 1\), respectively at room temperature. Both of these discoveries are based on the idea of confining the mean free path of phonon by reducing the dimension of the sample to 2D or even 1D which dramatically reduces the thermal conductivity without greatly affecting
the electronic transport. Basically, the sample is grown with a dimension which is smaller than the phonon mean free path but larger than the mean free path of charge carriers. Although these superlattices and nano structures show great potential for micro and nano scale thermoelectric applications, some of them require very high temperatures to achieve the reported ZT’s. Another class of thermoelectric materials is oxide thermoelectrics which are also being studied for potential thermoelectric thin films[41, 42] as well in bulk form[43].

2.6 Applications

All these efforts to improve efficiency (equation 2.3.17) of thermoelectric materials by optimizing the figure of merit (equation 2.4.2) show their importance for many applications. The fact that they can convert heat into electricity can be useful for applications in utilizing waste heat. The inverse thermoelectric effect (Peltier effect) discussed earlier shows their application in refrigeration as as heat pumps. One potential use of these materials is in automobiles, where waste heat from automobile exhaust can be used for recharging the car’s battery. This interconversion of heat and electricity can offer many other features for various items on the vehicle. Today car seats are available with thermoelectric heating and cooling. The ability to keep the beverages cold or hot has also been introduced in a few models using thermoelectric devices[44]. The idea to integrate a thermoelectric generator into the exhaust gas circulation cooler may become a reality if a material with ZT> 3.0 becomes available[45]. These materials would be useful for power generation in remote locations like space.

Thermoelectric thin films and nanostructures can be useful for on chip cooling in integrated circuits[46]. As low dimensional materials, they can be useful for systems which do not produce a lot of heat such as wireless sensor networks, mobile devices,
and medical applications[47]. Variety of thin film deposition techniques are used to develop relatively small thermoelectric devices by different companies[48, 49, 50, 51]. Similarly, bulk thermoelectric materials can be reduced[52] in size and possibly used for smaller scale thermoelectric applications.

2.7 Summary

This chapter presented a detailed explanation of thermoelectric effect, its significance for renewable energy applications, and brief introduction of current thermoelectric materials (bulk, thin films and nanostructures). There was also a discussion on efforts to optimize the performance in these materials. The potential of low thermal conductivity materials for a better thermoelectric performance was stated. In addition to studying low thermal conductivity materials, thermopower in these materials also need to be investigated. In the upcoming chapters, we will present our experimental technique for measuring in plane thermal conductivity, thermopower, and electrical conductivity for thin film as a function of temperature. We will also demonstrate how our technique enables us to measure all of these properties on one platform to minimize error in geometry and composition of sample.

The results of measured thermal conductivity of low stress silicon nitride (Si-N) bridges will be presented. The focus is on exploring amorphous silicon based thin films for their thermoelectric performance and our recent results will be presented in the later chapters.
Chapter 3

Thermal conductivity of micromachined low-stress silicon-nitride bridges from 77 to 325 K

3.1 Introduction

In the previous chapter, the dependence of figure of merit on three characteristic properties (thermal conductivity, thermopower and electrical conductivity) of a material was discussed. In thin films and nano structures, these properties need to be measured precisely in order to fully explain the thermoelectric behavior. This chapter provides detailed information about our robust experimental technique for in plane thermal conductivity measurement and we present our results of thermal conductivity measurements of 500 nm thick silicon nitride bridges.

In recent years, micro- or nano fabrication techniques have allowed advances
in both technical achievement and fundamental science. Many of the resulting devices are built using thin films, where thermal properties can often differ from bulk materials. For metals at high temperatures, $k$ is often estimated using the Wiedemann-Franz Law, which relates the electronic thermal conductivity to electrical conductivity for bulk metals where electrons dominate $k$. This law describes only the electronic transport and is valid over a wide range of temperatures for bulk samples. However, insulating or nanoscaled samples require measurements of thermal conductivity [53, 54, 55]. There are several well-established techniques for measuring the thermal properties of thin films in certain regimes, including the 3-$\omega$ method [56] and picosecond thermoreflectance [57, 58]. These predominantly measure the thermal conductivity in the direction perpendicular to the films supporting substrate often called the cross-plane thermal conductivity. As shown in Fig.3.1, we have designed a micromachined platform for thermal conductivity measurements using suspended SiN membranes which provide a strong, low-stress, electrically insulating substrate that is a fairly poor conductor of heat. Accurate knowledge of the thermal conductivity of this SiN is important because it is the single contribution to the background thermal conductance of our device. Similar SiN structures are also commonly used to thermally isolate sensitive thermal detectors, both bolometers and microcalorimeters, operated at low temperatures [59]. The thermal transport in these SiN films is often critical to optimal design of these devices. There is also fundamental interest in the thermal conductivity of this highly disordered material with strong covalent bonds [60, 61, 62].

In this chapter, I describe our experimental technique for measuring in-plane thermal conductivity of a wide range of thin films and present measured thermal conductivity of $\sim 500$ nm thick, low stress, Si-N bridges in the temperature range of 77 K to 325 K. By carefully controlling the geometry of the structure, we have dramatically reduced the radiation contribution to effective thermal conductance,
which often complicates steady state measurements of thermal conductivity at temperatures above 100 K. We also present the measurement of thermal conductivity of a metal by direct deposition of a 200 nm thick molybdenum sample thin film on the Si-N bridge and compare the results to the prediction of the Wiedemann-Franz law.

3.2 Device Fabrication

The fabrication process starts with a 3” (100) oriented Si wafer (Fig.3.2). A 500 nm thick layer of silicon-nitride is deposited on both sides of wafer the by low pressure chemical vapor deposition (LPCVD). This film is grown at 835°C, from 12 sccm of ammonia (NH$_3$) and 59 sccm of dichlorosilane (DCS), at a process pressure of 250 mTorr. The resulting low-stress film is silicon-rich compared to the stoichiometric composition (Si$_3$N$_4$). After the Si-N deposition, a 200 nm metal (Mo) layer is sputtered on the polished front side of the wafer and patterned into heaters and thermometers using standard optical lithography. Windows are etched in the Si-N layer via plasma etching (CF$_4$). Finally, the Si substrate beneath the patterned Si-N is removed using a KOH wet etch at 70°C for 5 hours. This releases the Si-N
Figure 3.2: Fabrication steps

structure leaving freely suspended islands (see Fig.3.1). Since the KOH etch stops only when a (111) plane of silicon meets the Si-N layer, the orientation of the islands, legs and bridge at 45° angles to the (100) direction allows these structures to be completely undercut by the anisotropic KOH etch. Fig.3.1(a) shows SEM images of two micromachined devices fabricated on a 1 cm x 1 cm Si-chip, taken after tilting the sample stage. In each device, two Si-N islands are suspended over a 2 mm x 2 mm etch pit via Si-N legs. In Device A there is no link between the islands, while in Device B a Si-N bridge bridges them. Fig.3.1(b) and Fig.3.1(c) are magnified views of the two devices.

3.3 Measurement Technique

Steady state measurements of thermal conductivity in this temperature range are often complicated by radiation losses (as described in chapter 1). For example, in
measurements of thin film thermal conductivity made with a micromachined membrane calorimeter[63], radiation contributes significantly to effective thermal conductance above 100 K. This was one of the main motivations for the development of the 3-ω method[56], which uses an ac technique to eliminate radiation effects. Though this technique is popular it is useful only above $\sim 30$ K, and almost exclusively measures in the direction perpendicular to the substrate. One goal of our design is to minimize radiation effects by significantly reducing the heated area of the device. Figure 3.3 shows thermal models of three different devices. Fig. 3.3(a) is the thermal model of Device A, where thermal conductance ($K_L$) occurs only through the legs when power ($P_h$) is applied to the heater on one of the islands. Fig. 3.3(b) shows a thermal model of Device B where a thermal conductance path ($K_B$) is added through the Si-N bridge connecting the two islands. Fig. 3.3(c) shows the thermal model of Device C where ($K_S$) shows the deposited sample thin film on the Si-N bridge which increases the thermal conductance through the bridge as compared to Device B.

The power dissipated in a device of type A as a function of temperature, $T_o$, is
Figure 3.4: a) Predicted $\Delta T$ vs $P$ for a simple model of the thermal platform that includes radiation losses at two temperatures, 95 K (upper lines) and 285 K (lower lines). Solid lines are calculated for a platform with a $(250 \mu m)^2$ heated area, dashed lines for a $(2.5 \text{ mm})^2$ heated area, and dotted line for no radiation contribution. The symbols represent measured values for Device A, which match the low radiation loss prediction extremely well. b) Predicted $K = P/\Delta T$ for the radiation models. The upturn caused by radiation losses would complicate thermal transport measurements for large-area platforms. *Inset:* Schematic of the simple thermal radiation model.
potentially affected by both conduction and radiation so that:

\[ P = \langle K_L(T_h, T_o) \rangle \Delta T + A_{\text{eff}} \epsilon_{\text{eff}} \sigma \left[ (T_o + \Delta T)^4 - T_o^4 \right], \]  

(3.3.1)

where the first term represents thermal conduction and is the average value of \( K_L \) between \( T_o \) and \( T_h \), \( \Delta T = T_h - T_o \), and the second term describes radiation emitted by the heated area of the device and absorbed from the environment. Here \( A_{\text{eff}} \) and \( \epsilon_{\text{eff}} \) respectively are the effective area and emissivity of the heated area of the device, and \( \sigma \) is the Stefan-Boltzmann radiation constant. Taylor expansion of the first term and simplification after keeping terms up to \( \Delta T^2 \) gives:

\[ P = \left( K_L(T_o) + 4A_{\text{eff}} \epsilon_{\text{eff}} \sigma T_o^3 \right) \Delta T + \left( \frac{1}{2} \frac{dK_L}{dT} \bigg|_{T_o} + 6A_{\text{eff}} \epsilon_{\text{eff}} \sigma T_o^2 \right) \Delta T^2 \]  

(3.3.2)

Therefore if radiation losses are significant, a plot of \( \Delta T \) vs. \( P \) will have a reduced slope and show somewhat increased curvature. An example using a simple model of a heated platform connected to a thermal bath via a single thermal link is shown in Fig. 3.4. In this model we consider thermal platforms with two different effective areas, but with the same emissivity (here chosen to be \( \epsilon = 0.05 \) as previously reported for similar micromachined devices[63]), and the same thermal link to the bath. In order to directly compare the predictions of Eq. 3.3.2 to our data, we used measured values of the thermal link, \( K_L \), and its first derivative for Device A, which will be discussed further below. Fig. 3.4a) shows the predicted \( \Delta T \) for a range of heater powers, determined from the positive root of Eq. 3.3.2 for two different temperatures. In addition to the two different areas, the curve with no radiation terms is shown. The modeled device with \( A = (2.5 \text{ mm})^2 \) leads to larger radiation losses, while the 100 times smaller area of our thermal platforms leads has no appreciable radiation loss. Fig. 3.4b) shows \( K = P/\Delta T \) vs. \( T_o \) that would result from the model
calculations. As seen previously in membrane nanocalorimeters with large heated areas, [63, 64] the radiation loss causes a pronounced upturn above 100 K. Use of such microcalorimeters for thermal conductivity measurements relies on correction for these radiation losses, which adds considerably to measurement errors.[63] The simple reduction in the size of the heated platform leads to only very small deviations from the zero-radiation limit. To directly test for radiation effects we perform a series of measurements on Device A which has two Si-N suspended islands but no Si-N bridge. Each island in this device is therefore a good approximation of the simple model used to estimate radiation losses above. As for the remaining measurements, we mount the device to the cold stage of a sample-in-vacuum cryostat on a Au plated copper sample holder, and ultrasonically wire-bond the device heaters and thermometers to a circuit board that provides connections to room temperature. The board and the device are covered with a radiation shield to provide an isothermal environment. Vacuum of $3 \times 10^{-6}$ Torr or better is maintained in the cryostat to prevent heat conduction through environmental gases around the sample holder and device.

Measurements with the thermal platform begin by regulating the temperature of the sample stage (and device frame) at $T_{\text{ref}}$. The maximum drift allowed for the reference temperature is 4 mK/minute. To calibrate the platform, we then measure the resistance of each thermometer using a 4-wire technique and a commercially available ac bridge while the sample stage temperature is controlled at $T_{\text{ref}}$. The maximum power dissipated in the thermometer while making these measurements is much lower than a nanowatt. The deviation of temperature on the device frame thermometer ($T_o$) is very small ($\approx 3$ mK) throughout the temperature range. Figure 3.3 shows the calibration curve for the frame thermometer of Device A. After this calibration step one of the islands is heated by applying a known current to the heater wire on the island. After heating, the temperatures on the frame, hot island
Figure 3.5: Example calibration of the micromachined thermometer, *Inset*: SEM micrograph of Mo wires patterned as thermometer and heater (the four wires used to measure each resistor are also visible)

and cold island are measured by again measuring the resistances. We also monitor the voltage drop on the heater to directly measure the applied power. We repeat this procedure for a series of heater currents, such that heater power is in the range of 0.2 $\mu$W to 17.5 $\mu$W while the power dissipated in each of the thermometer remains less than 1 nW. The standard deviation of the frame temperature, $T_o$, for all applied powers at sample stage temperatures, $T_{ref} = 77$ K, 149 K, and 299 K are $\pm2.72$ mK, $\pm3.90$ mK, and $\pm1.68$ mK, respectively. This very small standard deviation shows that the temperature of the device frame remains exceptionally stable during our measurements. Figure 3.3(a) shows a plot of the temperature on each of the islands versus power applied to the heater on one of the islands, at a constant reference temperature of 299 K for Device A. As the heater power increases, the temperature on the hot island also increases as expected. However, the temperature of the both the cold island and on the frame remains constant
Figure 3.6: Temperature vs. heater power at $T_{ref}=299K$ for a) Device A, and b) Device B. $T_o$ (x’s), $T_h$ (triangles) & $T_s$ (boxes) are the temperatures on frame, hot island & cold island respectively. lower right insets: optical image of devices, upper left insets: zoomed in regions for low heater power.
at the reference temperature ($T_{\text{ref}}$). We also verified that $\Delta T = T_{\text{hot}} - T_o$ as a function of power applied matches the prediction of the radiation model as shown in Fig. 3.3a). Both of these facts indicate that in this structure we have reduced the radiation contributions significantly. Since in Device A the legs form the only thermal link from the hot island to the thermal bath, thermal conductance through the legs is then calculated using,

$$K = \frac{P}{\Delta T} \quad (3.3.3)$$

where $P$ is the measured power and $\Delta T$ is the average temperature gradient across each leg of the hot island.

### 3.3.1 Thermal conductivity of Si-N bridge

When a Si-N bridge bridges the two islands, the thermal conductance is not only through the legs but also through the Si-N bridge, leading to the thermal model shown in Fig. 3.3(b), which is similar to that used to analyze measurements of thermal transport in nanostructures [55]. Fig. 3.3(b) shows a plot of temperatures on both islands and on the frame versus power at a reference temperature of 299 K for the Si-N bridge microstructure (Device B). In this case as the power applied increases on the hot island, the temperature on the cold island also increases by a small but clearly measurable amount as heat flows from the island along the bridge. The temperature on the frame ($T_o$) remains constant at $T_{\text{ref}}$. The rate of heat flow in the structure can be written mathematically as,

$$C_h \frac{\partial T_h}{\partial t} = -K_L(T_h - T_o) - K_B(T_h - T_s) + P_h \quad (3.3.4)$$

$$C_s \frac{\partial T_h}{\partial t} = -K_L(T_s - T_o) - K_B(T_s - T_h) + P_s \quad (3.3.5)$$
where $T_o$, $T_s$ and $T_h$ are temperatures on frame, cold island and hot island respectively. $C_h$, $C_s$, $P_h$ and $P_s$ are the specific heats and power dissipated on hot and cold islands respectively. $K_L$ and $K_B$ are thermal conductance through the legs and through the bridge. In a steady state measurement, the time dependent term vanishes and since we do not apply power to the cold island, we set $P_s=0$ which gives,

\[ 0 = -K_L(T_h - T_o) - K_B(T_h - T_s) + P_h \]  
\[ 0 = -K_L(T_s - T_o) - K_B(T_s - T_h) \]  

Solving these equation for $T_h$ and $T_s$ with $P_h = P$ gives,

\[ T_h = T_o + \frac{(K_L + K_B)P}{2K_B + K_L} \]  
\[ T_s = T_o + \frac{(K_B)P}{2K_B + K_L} \]

By fitting a straight line to the plot of $T_h$ and $T_s$ versus $P$, we calculate $K_B$ and $K_L$ from the slopes. Since we know the geometry of the bridge and the measured thermal conductance $K_B$ we determine,

\[ k_{Si-N} = \frac{K_B l}{w t}, \]

where $l$, $w$, $t$ are length, width and thickness of the bridge respectively.

### 3.3.2 Thermal conductivity of deposited thin films

In order to verify our experimental technique, we also present measurements of a device with a 200 nm thick Mo film sputtered on the Si-N bridge (Device C). The thermal conductance is measured using the same experimental technique described
above. In this case, the Mo adds a contribution to the bridge as shown in Fig. 3.3(c). A single subtraction of the background contribution to thermal conductance of Si-N ($K_{Si-N}$) gives the thermal conductance of our sample Mo thin film ($K_S$) and hence gives thermal conductivity of Mo ($k_S$).

$$K'_B = K_{Si-N} + K_S$$  \hspace{1cm} (3.3.11)

$$K_S = K'_B - K_{Si-N}$$  \hspace{1cm} (3.3.12)

$$k_S = \frac{K_S l}{w t}$$  \hspace{1cm} (3.3.13)

Here $l, w, t$ are length, width and thickness of the Mo film respectively.

### 3.4 Results and discussion

Figure 3.7 shows the thermal conductance through the Si-N bridge, $K_B$, and through the legs, $K_L$, for Device B. We see that $K_B$ is much lower than $K_L$ because the Mo wires deposited on the legs add a significant thermal conductance path. As we know the geometry of Si-N bridge between the islands, we use Eq. 3.3.10 to convert thermal conductance $K_B$ to thermal conductivity ($k$) of the Si-N bridge. Fig. 3.8 compares the resulting measured thermal conductivity of Si-N, $k_{Si-N}$, to previously reported amorphous Si-N films grown using LPCVD[60, 65],[61] and PECVD[62], as well as to vitreous silica (SiO$_2$)[66]. The high temperature values of our measured thermal conductivity of Si-N are in agreement with the earlier measurements of Si-N thin films. As the temperature drops, we see very little variation in our measured thermal conductivity of Si-N as a function of temperature. This is obviously a significant departure from the dependence seen in previously measured LPCVD Si-N films, and also deviates from the expected behavior in what we originally presumed was an amorphous film. The qualitative behavior of the measured and previously
Figure 3.7: Thermal conductance through the legs (Si-N+Mo) and through the Si-N bridge vs temperature, *upper left inset:* Thermal model, *lower right inset:* SEM micrograph of device.

Published data on Si-N is quite reminiscent of studies that compare thermal transport measured in both amorphous and polycrystalline allotropes of selenium and its alloys,[67, 68]. Note that the various LPCVD silicon-nitrides shown in Fig. 3.8 have different thicknesses, and this could also play a role in the microstructure of the film and/or its thermal conductivity. The variation in $k$ between the films grown with LPCVD and PECVD is also likely to be the result of different film microstructures.

The results of a preliminary investigation of the structure of several Si-N films all grown in the same LPCVD furnace under nominally identical conditions are shown in Figure 3.9. Here x-ray diffraction data were collected using a Bruker D8 Discover diffractometer with Cu x-ray tube excited at 35 kV and 30 mA. Cu $K_{\alpha}$ radiation was selected using an incident-bridge graphite monochromator. The incident bridge was collimated to the sample and data were collected using a 2-D multi-wire proportional detector. 2-D diffraction patterns were collapsed into the intensity vs.
Figure 3.8: Comparison of our measured thermal conductivity of Si-N ($k_{\text{Si-N}}$) with previously reported values for LPCVD Si-N (LP1[65], LP2[60]), and for plasma-enhanced CVD (PE[62]). Vitreous silica is shown for comparison ($\text{SiO}_2$[66]).

diffraction angle $2\theta$ 1-D traces for clarity by integrating over Debye rings ($\chi$ angle). The upper two plots, with apparent Bragg peaks at 13.8° and 20.3° indicate the likely presence of $\text{Si}_3\text{N}_4$ crystallites with a hexagonal crystal structure.[69] The position, and particularly the width of the peaks is affected by the exact Si-N stoichiometry, crystallite size, and possible residual stress in the films. The variation in Si-N peak widths from sample-to-sample (and the absence of peaks in some films) suggests variations in crystallite size and possible inhomogeneity both across a wafer and from run to run. Further structural characterization is required to discern the micro- or nanocrystalline nature of the Si-N.

The possibility of inhomogeneous crystallization of the Si-N film could present challenges for our thermal conductivity measurements, where we plan to use a reference bridge fabricated on the same 1 cm × 1 cm chip to measure the background contribution. The use of polycrystalline Si-N in the bridges offers no impediment
Figure 3.9: (Results of preliminary structural investigation using x-ray diffraction (the upper three data sets are shifted vertically for clarity). Small but well-defined peaks are seen in scans for Device B-1 and Device B-4. Peaks caused by the underlying silicon are also visible, except when the substrate was slightly misaligned. Scans of suspended Si-N islands with no metal features and of an unpatterned Si-N film did not show observable crystallite peaks, but this is most likely due to variation of crystallite size from run-to-run.
Figure 3.10: Comparison of results from three thermal platforms (of the Device B type) fabricated on a single Si wafer. a) Measured thermal conductances, $K_L$ shown above the axis break, and $K_B$ shown below. The large differences in $K_L$ are caused by thickness variation in the Mo leads that dominate the leg thermal conductance. b) Thermal conductivity of the Si-N forming the three bridges. Thicknesses were measured at several points on the frame of each platform by ellipsometry, the resulting error is approximately $\pm 3$ nm on each measurement. Devices B-1 and B-2 give very similar thermal conductivity, while Device B-3 is somewhat higher, but still within $\sim 10\%$ of the other values.
to this measurement scheme as long as large non-uniformities do not occur on these rather short length scales across the wafer. As shown in Fig. 3.10, thermal conductivity data on several bridges taken from different locations on a single wafer are closely grouped, with the worst deviation only as large as \( \sim 10\% \), suggesting that despite the possibility of inhomogeneity in the nano- or microstructures of the Si-N, the background contribution of the bridge is predictable, but should be periodically verified. The largest variation observed to date, for Device B-3, is most likely due to micro- or nanostructural inhomogeneity in the Si-N, but could also be related to moderate heating (several hours at temperatures between 150° and 200° C) during a previous experiment with this particular device. Though heating to these rather low temperatures (less than one-fourth the growth temperature, and an even smaller fraction of the expected melting temperature) would not normally significantly alter the structure of a film. However, since the thermodynamics of the silicon-nitride clearly requires further study, a partial low-temperature annealing can not be excluded.

Figure 3.11 compares the thermal conductance of the Si-N bridge with and without the 200 nm thick Mo sample film. At these temperatures, addition of the metal film simply adds to the total thermal conductance of the bridge, resulting in the top curve in Fig. 3.12. Subtracting the previously measured thermal conductance of the bridge \((K_{Si-N})\) isolates the contribution of the Mo film, which in this case is large compared to the background of the bridge. The known geometry of the film allows determination of the measured thermal conductivity of the Mo. The resulting thermal conductivity is shown in Fig. 3.11, which also demonstrates the accuracy of our experimental technique of measuring thermal conductivity of thin films. Since measurement of the temperature of each island involves measuring the resistance of each Mo thermometer as a function of temperature, resistivity and electrical conductivity of Mo as a function of temperature are easily determined us-
Figure 3.11: Comparison of thermal conductance $K_B$ with $K_{S(Mo)}$ after background subtraction $K_{S(Mo)} = [(K_{Si-N+Mo})-(K_{Si-N})]$, upper left inset: Optical picture of device, lower right inset: Thermal model.

Figure 3.12: Thermal conductivity of Measured $k_{S(Mo)}$ compared with measured $k_{Si-N}$ and Wiedemann-Franz $k_{WF(Mo)}$ (divided by a scale factor 1.05)
ing the known geometry of the resistors. Fig. 3.12 compares our measured thermal conductivity of Mo, $k_{S(Mo)}$, determined from Eq. 11-13, with the Weidemann-Franz thermal conductivity of $k_{WF(Mo)}$. The measured data matches extremely well with the Wiedemann-Franz thermal conductivity after introducing a scaling factor of 1.05. This slight difference between $k_{S(Mo)}$ and $k_{WF(Mo)}$ is most likely caused either by a small deviation in the sample geometry due to a thickness variation, or by a slightly different Lorenz number.

3.5 Conclusion

We presented thermal conductivity measurements of micromachined low-stress Si-N bridges and Mo thin film from 77-325 K. Near 300 K our results match earlier measurements of thermal conductivity of Si-N, and at lower temperatures show behavior similar to polycrystalline materials. X-ray diffraction indicates the presence of Si$_3$N$_4$ crystallites, suggesting that this material, which was presumed to be amorphous due to similar growth conditions as used for previously reported Si-N, has a more ordered structure that leads to significantly different thermal transport. Despite the deviation from the amorphous material, the Si-N bridges have very similar thermal conductivities across a wafer. The measured thermal conductivity of a 200 nm thick Mo thin film agrees well with the prediction of the Wiedemann-Franz law. We are in the process of fabricating thermal platforms with different thicknesses of Si-N to check a possible thickness dependence, are beginning a more detailed investigation of the structure of the Si-N, and are also working to understand the physics of the Si-N bridges at low temperatures by fabricating platforms with semiconducting thermometers. We would like to thank J. A. Beall, G. C. Hilton, and K. D. Irwin for many helpful discussions and other contributions, D. Balzar for the XRD scans and assistance in interpretation, D. Queen for general discussions of silicon-nitride,
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Chapter 4

Study of long wavelength phonons surface scattering in low stress silicon nitride bridges

4.1 Introduction

Thermal conduction in solids is governed by several mechanisms and there are many processes which limit the effectiveness of each mechanism. When atoms vibrate in a material they cause heat transfer. This type of thermal conduction is found in non-metals and insulators. In metals, although the lattice (atomic) vibrations do play a role in heat transport but the thermal conductance is dominated by electrons. The lattice vibrations, phonons, can be very sensitive to the structure of the material under consideration. For example, dramatic changes in the thermal conductivity of silicon has been observed due to structural changes as well as due to the sample size reduction\[5, 40\]. In this chapter, I will discuss thermal conductivity measurements of 500 nm thick, 806 µm long, and 35 µm wide low stress
suspended Si-N bridges and the effect on the thermal conduction of Si-N caused by surface variation of Si-N bridges. Several experiments were conducted in order to understand the surface effects in Si-N membrane which is important to perform further experiments for thermal conductivity measurements of thin films.

4.2 Lattice Vibrations: Phonons

The aim of this section is to establish an understanding of modes of vibrations in a solid. The atomic vibrations in a crystal carry energy in the form of a wave due to interaction with each other. The energy of lattice vibration is quantized, and each quantum is called phonon. According to the Debye model, the atoms in a solid vibrate within a range of frequencies with a high frequency cutoff called Debye frequency, $\omega_D = \frac{6\pi^2 N v^3}{V}$, which is determined for fixed number of vibratory modes (N) per unit volume and $v$ is the velocity of sound. Using the dispersion relation which relates the frequency of vibration to the wave vector as $\omega = vK$, the group velocity, $v_g = \frac{d\omega}{dK}$ can be determined[70]. Group velocity of the energy carried by phonon during their propagation through the medium.

A wavevector, $K$, represents a traveling wave and it polarizes along the direction of propagation which is related to the structure of the crystal and number of atoms per primitive basis. Depending on the mode of polarization for a given propagation direction, the frequency in the dispersion relation develops two branches. This is often referred as modes of vibrations, acoustic and optical.

Phonons in the acoustic mode have smaller frequencies in the long wavelength limit and are called acoustic phonons. On the other hand, optical phonons lie at the higher frequency and disperse less (as shown in Figure 4.1).

Referring back to the Debye frequency, a cut off wave vector $K_D$ is determined
Figure 4.1: Optical and Acoustic modes. Optical modes lie at higher frequencies and show less dispersion than acoustic modes. The general expression for limiting frequencies can be obtained by choosing appropriate value of wave vector, \(k\).

\[ K_D = \frac{\omega_D}{v} = \left(\frac{6\pi^2 N}{V}\right)^{1/3} \]  

(4.2.1)

where \(v\) is the velocity of sound, \(N/V\) is the number of atoms (or the total number of acoustic phonon modes) in a given unit volume. In Debye model, the modes of vibration are not allowed to have a wave vector greater than \(K_D\). When the atoms vibrate due an increase in temperature, there is a temperature at which the crystal vibrates with its highest mode of vibration. This temperature is called Debye temperature (\(\theta_D\)). Mathematically, it is expressed as,

\[ \theta_D = \left(\frac{h v}{k_B}\right)\left(\frac{6\pi^2 N}{V}\right)^{1/3} \]  

(4.2.2)

The Debye heat capacity is derived using the Debye temperature and the total

\[ 42 \]
phonon energy\cite{70}. The Debye heat capacity, $C_v$ is expressed as,

$$C_v = 9k_B\left(\frac{T}{\theta_D}\right)^3 \int_0^{\theta_D} \left(\frac{\hbar \omega}{k_B T}\right)^4 e^{\frac{\hbar \omega}{k_B T}} \frac{1}{e^{\frac{\hbar \omega}{k_B T}} - 1} \, d\omega$$

(4.2.3)

In equation 4.2.3 we see that the heat capacity has a strong dependence on the ratio of the absolute temperature ($T$) to the Debye temperature ($\theta_D$). We can then characterize heat capacity in the two temperature limits,

(i) High temperature limit, $T \gg \theta_D$

(ii) Low temperature limit, $T \ll \theta_D$

Heat capacity indicates how much thermal energy a physical system can absorb with the change in temperature ($T$). According to the Debye model, in the high temperature limit the molar heat capacity saturates at the classical value of $3Nk_B$ when plotted as a function of $\frac{T}{\theta_D}$ and becomes independent of temperature. The high temperature heat capacity in solids is also explained by Einstein model which assumes that the each atom in a solid vibrates independently with the same frequency\cite{71, 70}. This model fits very well with experimental data in high temperature limits but the approach is simple and only applicable at low temperature. The Debye model explains the low temperature limit as the heat capacity decreases with the third power of temperature. At these temperature, only low frequency (long wavelength) acoustic phonons (having energy $\hbar \omega < k_B T$) can be excited. Phonon mean free path increases with decreasing temperature so does the heat capacity decreases as $T^3$. These results show good agreement with many experiments but this low temperature approximation fails at significantly low temperatures for high frequency (short wavelength) modes.
4.3 Thermal Conductivity and Phonons

Thermal transport in a solid is characteristic to a material under consideration, its structure, thermal history, and in some cases dimension of the material[5, 40]. The aim of the previous discussion of Debye heat capacity and heat conduction due to phonons leads us to the thermal conductivity concept. According to the kinetic theory of gases, thermal conductivity, \( k \), is mathematically expressed as,

\[
k = \frac{1}{3} C v l
\]  

(4.3.1)

where \( C \) is the heat capacity, \( v \) is the velocity of sound and \( l \) is the phonon mean free path.

Equation 4.3.1 shows that thermal conductivity is directly proportional to the velocity of sound which does not change very much in a material but it can only differ slightly in very dense materials. However, heat capacity has a standard temperature dependence discussed earlier in this section. There is no explicit temperature dependence on thermal conductivity in equation 4.3.1 but the temperature dependence appears through the phonon mean free path, \( l \) which is inversely related with temperature (\( l \propto 1/T \)) at high temperatures because the number of phonons is proportional to the temperature in crystals due to anharmonicity at high T. Phonon mean free path follows the same temperature dependence at low temperatures as well because availability of thermal energy. In non crystalline solids such as vitreous silica in low temperature limit, the phonon mean free path varies as \( 1/T^4 \) because of elastic scattering through impurity atoms or vacancies[72].

Phonons do not carry a physical momentum but they carry heat along the material by interacting with other phonons, defects or impurity sites, or with electrons (in the case of metals). The first two interactions are more frequent in amorphous solids and insulators where the number of defect sites are greater and phonons are
the only contribution to the thermal conduction. When phonons propagate through a material, their mean free path can be limited by the interactions with defects and with the boundary or surface of the sample. When phonons are thermally excited, they come to thermal equilibrium by various scattering mechanisms\[3\]. These scattering processes may be elastic or inelastic in nature and hence affects the heat transport in the material. The two main phonon scattering processes are:

(i) *Umklapp Process* or (U-Process): is a phonon-phonon scattering process and could be electron-phonon scattering in metallic solids. In this process, when two phonons interact, one of them scatters off in a different direction and hence the total energy of the system is not conserved. This causes a thermal resistance and reduces the thermal conductivity. Phonons can also be scattered from the defects cites or from the surface of the sample. This type of scattering also causes a reduction in thermal conduction because it tries to restore the thermal equilibrium of the system by giving rise to thermal resistance\[3\].

(ii) *Normal Process* or (N- Process): is also a phonon-phonon, phonon-impurity or phonon-electron scattering process. In this process, the interaction is elastic and energy remain conserved. This process do not give rise to thermal resistance but contribute to the heat energy transfer within the sample by interacting with other phonon modes. This process prevents large deviation from thermal equilibrium.

## 4.4 Surface Scattering and Thermal conductivity of Si-N at Low Temperature

When a phonon scatters off the surfaces of a sample it can keep moving with the same energy and its mean free path keep increasing. This type of scattering is called specular scattering. On the other hand if the phonon diverts in a different direction after interaction then it’s mean free path shortens which affects the heat energy
transfer in a negative way, this type of scattering is called diffuse scattering[63]. The surface or boundary scattering is a phenomenon which is usually observed at low temperatures when the phonon mean free path increases and becomes a function of the dimension of the sample, causes a decrease in thermal conductance. The phonons in acoustic modes are low frequency phonons and are also referred as long wavelength phonons which cause a change (decrease) in thermal conductance when they are involved in diffuse scattering from the sample surface.

The material under investigation is the low stress Si-N membrane. The effect of long wavelength phonons on thermal conductance of Si-N membrane was reported at low temperatures by Holmes[61]. In this experiment, sub micron size Ag epoxy in acetone was distributed onto the surface of a 1 μm thick Si-N membrane and let the solvent to evaporate. This was to contaminate the surface. The thermal conductance was measured before and after the Ag particles introduction on the Si-N surface. A decrease in thermal conductance was observed below 4 K due to diffuse phonon surface scattering after the introduction of surface roughness. A significant decrease in thermal conductance was also observed when the width of the sample was decreased by a factor of 2 and thermal conductance dropped by a factor of 10[61]. A reduction in thermal conductance has also been observed in similar type of experiments for crystalline insulators when the surface is varied via thin film deposition[73, 74]. Another recent measurement of thermal conductivity of a-Si:H also show a strong phonon mean free path dependence on thermal conductivity[75]. All these results suggest the sensitivity of thermal conductivity on the propagation of phonons in the material and on phonon scattering mechanism. The question which arises that is this diffuse scattering mechanism limited to low temperature regime? The heart of our experimental technique for measuring in plane thermal conductivity of thin films (discussed in chapter 3) is the micromachined low stress silicon nitride based thermal isolation platform (insets of Figure 4.6). Since the Si-
N is the only background contribution to the total measured thermal conductance, it is very important to consider all possible factors which can affect the thermal conductance through Si-N membrane. In the later sections of this chapter, I will discuss the decrease and variation in measured thermal conductance (and thermal conductivity) through several Si-N bridges in the temperature range of 77-325 K.

4.5 Thermal Conductivity of Silicon Nitride (Si-N)

4.5.1 Thermal Conductivity measurements 500 nm thick Si-N membranes

We measured thermal conductivity of several 500 nm thick suspended Si-N bridges as a function of temperature. This Si-N membrane is grown with Low Pressure Chemical Vapor Deposition (LPCVD). The silicon rich Si-N is a low stress membrane and has been used to fabricate suspended structure for microcalorimetry to study fundamental properties of thin films\cite{64, 63, 76, 77, 78}.

Our initial measurements of thermal conductivity of Si-N bridges and the measurement technique is described elsewhere\cite{79}. Thermal conductivity is an intrinsic physical property which is a characteristics of the material itself but there are factors\cite{80} which can affect the intrinsic nature of it. We measure thermal conductance through 500 nm thick, 806 \(\mu\)m long, and 35 \(\mu\)m wide Si-N bridges and using these dimensions to convert the thermal conductance into thermal conductivity. One of the best part of our measurement technique is that there is no background subtraction to the thermal conductance of Si-N bridge. Figure 4.2(a) shows the measured thermal conductivity of from the first set of fabricated platforms. We see that there is a \(\pm 3\%\) variation around room temperature in the measured thermal conductivity of Si-N bridges across the wafer (Figure 4.3) and about \(\pm 13\%\) at low temperature end. One reason of this range of thermal conductivity values could be
Figure 4.2: (a) Thermal conductivity measurements of 500 nm Si-N bridges from across the wafer 1 (ref:4.3), (b) Thermal conductivity measurements of 500 nm thick Si-N bridges taken from another wafer and fabricated with wide leads to measure thermopower, inset: SEM micrograph of the thermal isolation platform, both wafers have Si-N membranes which are grown by LPCVD at NIST.
the thickness variation of Si-N membrane across the wafer. In Figure 4.3, the color difference in the membrane across the wafer suggests thickness variation. Light reflects at different angles from the transparent surface of Si-N because of thickness variation on the surface. In Figure 4.2(a), the data plots shown with * were measured in a different low temperature cryostat (see Figure 4.6) but all other measurements are done in the liquid nitrogen cryostat shown in Figure 4.4. The measurement technique is exactly the same for all these measurements (described in details in chapter 3). The other factors which may cause this deviation will be discussed later in this chapter. The data reproducibility and repeatability of our measurement technique has be tested and proven several times. When there is no physical change in the measured thermal conductance of a bridge we get very repeatable results. One example of data repeatability and reliability is shown in Figure 4.5.

Each fabricated chip has two platforms which are marked as UR (Upper Right) and LL (Lower Left). In Figure 4.3, each of the columns in wafer were assigned letters A through E and rows were assigned numbers 1 through 6. This naming scheme helps us to determine that the measured Si-N bridge was taken from which part of the fabricated wafer. The legends in the Figure 4.2, 4.7 & 4.8 follow this naming scheme.
Figure 4.4: Our liquid nitrogen cryostat in which almost all of our measurements are done.

Figure 4.5: Compares the measured thermal conductance of a Si-N bridge measured several times. When the thermal conductance does not change physically we get very repeatable results and this is an example of data reliability.
Figure 4.6: (a) An image of He-3 Fridge, which was used to measured three Si-N bridges shown with * in Figure 4.2, (b) Close up view of the delicate electronics in the He-3 cryostat where sample is installed for measurement.

Figure 4.2b shows thermal conductivity measurements of several Si-N bridges fabricated at a different time. In Figure 4.2b, the thermal conductivity values varies within ± 6 % at room temperature and about ± 4 % at low temperature end. This deviation in thermal conductivity at low temperature end is relatively smaller as compared to the measured values in Figure 4.2a. The method of growth of these Si-N membrane suggest an amorphous structure but a preliminary X-ray diffraction analysis, described in chapter 2, shows that these membranes maybe micro-nano crystalline in nature[79]. The size of Si$_3$N$_4$ crystallites could further be determined by detailed TEM image analysis. The local micro-nano crystalline nature of a material can also cause a random variation in thermal conductivity[81]. As it has been discussed in previous section of this chapter that thermal conductivity is very sensitive to how phonon propagate through the material, especially, in insulators. The important point to note here is that although the numbers for thermal conductivity
are slightly different but the behavior as a function of temperature is same for all these measurements.

Figure 4.7a and Figure 4.8a shows thermal conductance through the Si-N bridges and 4.7b and Figure 4.8b shows thermal conductance through the legs of the thermal isolation platforms. The thermal conductance through legs is dominated by metal (Mo) leads but the slight variation could come from the variation in thermal conductance through the Si-N membrane, thickness variation in metal layer or possibly the phonon scattering at the metal-insulator (Mo-Si-N) interface. The deviation in thermal conductance of Si-N follows the same pattern as we see for thermal conductivity in Si-N membrane in Figure 4.7a & b. The error bars on each of these thermal conductance measurement is $\sim 4 \times 10^{-4} \mu \text{W/K}$ at low temperature end and $\sim 1 \times 10^{-3} \mu \text{W/K}$ at high temperature end (see Appendix A for error bar calculations). In the next section, I will discuss different experiments that were performed to establish an understanding of this variation in measured thermal conductance (conductivity) in our Si-N bridges, the possible causes, and the physics behind it.

4.6 Motivation to study Surface scattering in Si-N membranes is temperature range of 77-325K

Thermal conductance through Si-N membranes are affected by increasing the surface roughness in the low temperature limit[61]. The motivation to test this phenomenon at high temperature came from the fact that in some cases when we deposited a low thermal conductivity thin film (such as, $a$-Si and $a$-Si alloys) thin film on the Si-N bridge, we did not see the the expected contribution of the film to the total measured thermal conductance and in some cases the total thermal conductance was lower than the pre-measured thermal conductance of Si-N. There can be more than one reason for this to happen, either the deposited film is not in good ther-
Figure 4.7: (a) Thermal conductance through of Si-N bridges from across the wafer (ref: Figure 4.3). The measurement shown with * were measured in a low temperature cryostat (Figure 4.6). Upper right inset: Optical image of the thermal isolation platform, (b) Thermal conductance through legs (Si-N + Mo leads) shows deviation which could be from the thickness variation of metal layer in combination with the variation in Si-N.
Figure 4.8: (a) Thermal conductance measurements of sixteen Si-N bridges taken from a single wafer and fabricated with wide leads to measure thermopower (inset: SEM micrograph of the thermal isolation platform). This Si-N membrane is also grown with LPCVD at NIST, (b) Thermal conductance through legs (Si-N + Mo leads).
mal contact with the Si-N surface or the background thermal conductance ($K_{Si-N}$) changed after or during the film deposition. The first case is less probable because if the deposited film is not in good thermal contact the total thermal conductance can not be lower the actual background unless the deposition of the films changes surface of Si-N bridge or it has already been changed over time (I will discuss this issue again later in this chapter). The case of changing the background thermal conductance ($K_{Si-N}$) leads us to test the long wavelength phonon diffuse surface scattering in our micromachined Si-N bridges. When long wavelength phonons are involved in diffuse surface scattering which is an inelastic scattering process, they can get scattered in an opposite or different direction which reduces the energy they carry with them. This could result in decreased thermal conductance. In order to test this phenomenon at relatively high temperatures (77-325 K), we performed a series of experiments which will be discussed next.

4.6.1 Deposition of 5 Å (0.5 nm) of Au on Si-N

We introduced surface roughness in our Si-N membrane in a similar manner as previously done by gluing the sub-micron Ag particles on the membrane[61]. We deposited a 5 Å (0.5 nm) discontinuous layer of Au by e-beam evaporation onto two Si-N bridges. When we deposit a film on the Si-N bridge we also deposit it on Si-N coated substrate for other studies on the films (e.g, structural analysis, thickness measurement etc). The discontinuity of the Au film was verified by measuring electrical resistance on the substrate which was infinite. The thermal conductance through these bridges were measured before and after the Au deposition. Figure 4.9(a) compares the measured thermal conductance before and after 5 Å of Au deposition for one of the bridges. We can clearly see a 2% drop in thermal conductance in $K_{Si-N}$ in the temperature range of 77 to 125 K shown with a solid line. The measured $K_{Si-N}$ after the Au deposition does not lie within the error bars indi-
cating that this is a significant change in thermal conductance to the best of our knowledge. The sensitivity of our measurement enables us to be able to detect these small changes in thermal conductance. The error in our thermal conductance measurement is less than 1% throughout the entire temperature range. Figure 4.9(b) shows the measured $K_{Si-N}$ of second Si-N bridge after 5 Å of Au deposition and the drop the in $K_{Si-N}$ is 3% all the way from 77 to 250 K. The decrease in $K_{Si-N}$ which is observed after Au deposition suggests some variation in phonon propagation through the Si-N membrane but this needs to verified by performing more measurements. It is important to mention here that the time elapsed between the $K_{Si-N}$ measurements of the bridges before and after Au deposition is a month. It is not out of question that the some surface variation of Si-N might have been occurred while the bridge was exposed to atmospheric pressure for a given amount of time. It is important to consider the time dependent variation in $K_{Si-N}$ because if the long wavelength phonons surface scattering is responsible for this decrease when the surface of Si-N is rough then any non intentional change in the surface may also activate this decrease in $K_{Si-N}$. In order to verify this we performed an other experiment which is discussed next.

4.6.2 Thermal Conductance through Si-N bridge as a function of Time

In order to investigate whether the thermal conductances of Si-N is affected by the fact that they are stored at ambient pressure after fabrication, we measured thermal conductance of a Si-N bridge and stored it in a clean ambient environment for a month. After a month it was measured again. Figure 4.10 compares two thermal conductances of the same bridge when the time elapsed between two measurements is 4 weeks. We see a 3 % decrease in the measured values which lies outside the error bars. In this case no intentional surface roughness (or variation) was introduced ex-
Figure 4.9: (a) solid circles Measured $K_{Si-N}$ through 806 $\mu$m bridge before Au particles deposition, open squares $K_{Si-N}$ after deposition, (b) solid circles Measured $K_{Si-N}$ through the second 806 $\mu$m bridge before Au particles deposition, open squares $K_{Si-N}$ after deposition.
cept that the Si-N bridge was left at atmospheric pressure for a certain time period. This suggests that the atmospheric reactions with the Si-N bridge surface replicated the surface variation which we introduced in the earlier experiment by depositing 5 Å (0.5 nm) of Au. As it has been mentioned in earlier chapters that these thermal conductance measurements are always done when a vacuum of 7 x 10⁻⁷ Torr (= 9.3 x 10⁻⁵ Pa) is maintained throughout the measurement. The measurement of K_{Si−N} on this bridge was repeated for the data reproducibility and reliability which we do periodically. The results match well with the second time measurement, shown in Figure 4.10b. To continue testing the time dependent change in the measured thermal conductance, we left this bridge in a clean environment at atmospheric pressure for another month and then measured it again. No change in measured thermal conductance of Si-N (K_{Si−N}) was observed this time and shown in Figure 4.12. Thermal conductance through another pre-measured Si-N bridge was re-measured after four months. Figure 6.3 shows a 12 % decrease in K_{Si−N} in the temperature range of 77- 150 K but lesser above 150 K. This is a Si-N bridge which showed the highest thermal conductance among all the Si-N bridges we measured and is shown as ‘D1LL’ in Figure 4.8a. These evidences of decrease in thermal conductance through Si-N bridges suggest that the thermal transport in these Si-N bridges is somehow altered over time and with the increase in surface roughness. These changes are comparable to the initial values of measured thermal conductance (K_{Si−N}). The effect of phonon diffuse scattering to the sample boundary is usually responsible for this act but how and why the surface is changing in this Si-N membrane is an open question which will be addressed in the later sections. Our results show that there is a dependence of K_{Si−N} on the surface of Si-N which is more prominent in the relatively low temperature range from 77- 150 K. Therefore, the open questions are how long does it take in the atmosphere for the Si-N bridge to alter its surface and how much variation can occur in that time period? When
Figure 4.10: Time dependent change in thermal conductance of Si-N. (a) Thermal conductance through a Si-N bridge measured twice when the time elapsed between two measurements was 5 weeks, (b) Thermal conductance through a Si-N bridge measured again for reproducibility.
Figure 4.11: Measured thermal conductance of the Si-N bridge twice when the time elapsed between two measurements is four months. A significant decrease is observed in over a four month time period (shown in Figure 6.1a) after deposition of a $\sim 35 \text{Å}$ of more Au of the bridge.

is the surface varied enough to saturate the long wavelength phonon causing diffuse scattering? To answer all these questions we have to do more testing.

### 4.6.3 Deposition of Series of Au thicknesses on a single Si-N bridge

In this experiment, we study the effect of the thickness of deposited film on the thermal conductance of Si-N. We picked a Si-N bridge which shows a highest thermal conductance when it was measured first time. It is the A3LL plot in Figure 4.8a. The bridge of highest thermal conductance was picked to determine the percent change in thermal conductance (if there is any) after we intentionally make the surface of the Si-N bridge rough. This was done by depositing a 10 Å of discontinuous layer of Au on the Si-N bridge. Figure 6.1a shows the thermal conductance of the Si-N bridge before and after 10 Å of Au deposition. As mentioned earlier, when we deposit a film on the bridge, we also deposit it on a Si-N substrate. The discontinu-
Figure 4.12: Thermal conductance of the same bridge (shown in Figure 4.10a & b) measured again after four weeks.

ity of the Au layer was confirmed in two ways: (i) AFM analysis of the Au surface on the substrate, shown in Figure 6.1b and (ii) by measuring the electrical resistance on the substrate which was infinite in case of a discontinuous film. In Figure 6.1a, we see a significant decrease in $K_{Si-N}$ after 10 Å of Au deposition. This decrease in $K_{Si-N}$ is analogous to the results we saw for D1LL Si-N bridge (discussed in previous section) where no intentional surface roughness was introduced.

The decrease in $K_{Si-N}$ after after 10 Å of Au deposition is about 13 % in the temperature range of 200 to 325 K but about 18 % in the temperature range of 77- to 199 K. The thermal conductance of this bridge was measured several times after Au deposition and reliability of our measured data was confirmed which is shown with open circles in Figure 6.1a. We then deposited a $\sim 35$ Å (3.5 nm) Au on the top of 10 Å (1 nm) Au on the same bridge and measured the thermal conductance again. This time total measured thermal conductance increases and shows a good contribution to the thermal conductance of Si-N by the deposited Au film. Figure 6.2 shows $K_{Si-N}$ and its variations as a function of the deposited
Figure 4.13: Increasing surface roughness of the membrane: Measured thermal conductance through a 806 $\mu$m bridge before and after the deposition of a 10 Å (1 nm) discontinuous layer of Au (b) Discontinuity of the film was verified by AFM surface analysis of 10 Å (1 nm) of Au.
Figure 4.14: Measured thermal conductance of the Si-N bridge (shown in Figure 6.1a) after deposition of a \( \sim 35 \, \text{Å} \) (3.5 nm) of more Au of the bridge

Au film thickness. To calculate the thermal conductivity of the Au film, the thermal conductance of Si-N (with 10 Å of Au) was used as a background subtraction which is equal to \( K_{Au} = (K_{Si-N} + K_{35ÅAu}) - (K_{Si-N} + K_{10ÅAu}) \). The measured thermal conductance is then converted to thermal conductivity, \( k_{Au} = \frac{K_{Au} \cdot wt}{l} \), using thickness, \( t=45 \, \text{Å} \) of deposited Au film (the thickness of previous 10 Å Au is also considered) and where \( w=35 \, \mu\text{m} \) and \( l=806 \, \mu\text{m} \) are the width & length of the bridge, respectively. The measured room temperature thermal conductivity of Au is 2.08 W/cm K whereas the Wiedemann-Franz law \( (k/\sigma = LT) \), where \( L \) is the Lorenz number) prediction of thermal conductivity of the deposited film (using the measured room temperature resistance) is 2.36 W/cm K. The difference between predicted and measured thermal conductivity of Au film is \( \sim 12 \% \). This result suggests that the background subtraction of the thermal conductance was close to the correct background but it also possible that the thermal conductance of Si-N varied more during or after the deposition. If the long wavelength phonons are causing the decrease in thermal conductance when the Si-N surface is rough, their
effect should saturate as soon as the deposited film becomes continuous. To verify this behavior we deposited a 1000 Å (100 nm) of Au on the same bridge and thermal conductance as a function of temperature was measured. Figure 6.4a compares thermal conductance before and after a series of Au film deposition. To determine the contribution of 1000 Å (100 nm) Au to the total measured thermal conductance, we subtracted out the thermal conductance shown with curly brackets in 6.4a as background. In Figure 6.4b, measured thermal conductivity of Au is compared with predicted Wiedemann-Franz thermal conductivity from measured resistivity as a function of temperature. The measured thermal conductivity of Au film is \( \sim 90\% \) in agreement with predicted \( k_{WF} \). This result shows that a proper background subtraction of the thermal conductance significantly improves the precision of the thermal conductivity measurement of thin films. The Wiedemann-Franz law works well for bulk metals, it is possible that deposited Au has not reached its bulk limit. The thickness of the film and the variation is Lorenz number may also cause this discrepancy between the measured and predicted thermal conductivity.

4.6.4 Hydrogenation of Si-N membrane

One reason of this surface variation could be related to the the KOH etch used to release the thermal isolation structure. To fabricate these suspended thermal isolation platforms, the last fabrication step is to etch the Si under Si-N membrane using wet KOH etch to form these suspended structure. This silicon nitride membrane is grown as silicon rich to have low stress membrane[82, 83]. In the KOH etch, it is possible that some of the Si on the Si-N surface is etched and leave few dangling bonds on the surface. A detailed surface analysis is necessary before and after the KOH etch to establish this argument. Silicon dangling bonds may react with oxygen in the air and vary the surface chemistry or introduce surface roughness which causes a decrease in thermal conductance. Dangling bonds also like to bond with H\(_2\).
Figure 4.15: Total thermal conductance after 1000 Å (100 nm) of Au deposition compared with thermal conductance in all previous depositions of the same bridge, b) Measured thermal conductivity of 1000 Å (100 nm) of Au compared with predicted WiedemannFranz thermal conductivity of Au from measured resistivity. There is \sim 90 \% agreement in measured and predicted values of $k_{Au}$.

65
atoms. In our UHV e beam evaporation chamber where the thin films are deposited, 
H\textsubscript{2} is usually present during the deposition due to the out gassing of electron gun. 
A Si-N bridge stays in UHV chamber for some time (with sample shutter closed) 
while the desired rate of the evaporating material is being achieved. During this 
time some hydrogen is always present in the chamber which is seen on residual gas 
analyzer. If the surface of Si-N has some dangling bonds, they might find this H\textsubscript{2} 
to attach with.

To see if there is any surface variation occurs during the deposition because of 
presence of H\textsubscript{2} gas in the chamber, we picked a Si-N bridge (shown as D1LL in Fig-
ure 4.8a) which showed a significant reduction in thermal conductance over a four 
months period (discussed in earlier sections). This bridge was hydrogenated for an 
hour in the chamber where the total pressure was dominated by the H\textsubscript{2} pressure 
$\sim 3.2 \times 10^{-6}$ Torr ($=4.2x10^{-4}$ Pa). Thermal conductance through the bridge was 
measured again and no change was observed. If the surface of Si-N stabilizes over 
a time period then the thermal conductance would not change further which might 
be the reason of no change in this case. A detailed surface analysis may give some 
more information about the surface of Si-N bridges.

### 4.6.5 Measured thermal conductivity of Alumina (Al\textsubscript{2}O\textsubscript{3})

In order to verify the effect of thin film deposition on the thermal conductance of 
Si-N and on the accuracy of the measured thermal conductivity of the deposited 
film, we deposited a 100 nm (1000 Å) alumina film (which is a low thermal conduc-
tivity film) on a pre-measured Si-N bridge and measured the thermal conductance 
after film deposition. Figure 6.5a compares the total measured thermal conductance 
after 100 nm of alumina deposition, thermal conductance through Si-N bridge, and 
the thermal conductance of 100 nm alumina after subtraction. The thermal con-
ductance is then converted into thermal conductivity shown in Figure 6.5b and is
Figure 4.16: a) Total measured thermal conductance after a 100 nm of alumina deposition compared with Si-N background and the thermal conductance through 100 nm Alumina after subtraction, b) Measured thermal conductivity of alumina compared with thermal conductivity of Si-N and the literature value of $k_{\text{alumina}}$ [84]. Our measured thermal conductivity is lower than the previously reported data which could be because of background variation after the film deposition. In the process of identifying the correct background subtraction, we deposited another 200 nm (2000 Å) of alumina compared with $k_{\text{Si--N}}$ and with literature value of $k_{\text{alumina}}$ [84].
Figure 4.17: a) Total measured thermal conductance after a 200 nm of alumina deposition compared with Si-N background and the thermal conductance through 200 nm Alumina after subtraction. b) Measured thermal conductivity of alumina in two depositions is compared with \( k_{Si-N} \) and the literature value of \( k_{alumina} \)\[84\].

on the top of 100 nm alumina and thermal conductance was measured. To find the thermal conductance through freshly deposited 200 nm alumina film we used the \( K_{(Si-N+100nmAl_2O_3)} \) as the background subtraction (shown in Figure 6.6a). Figure 6.6b compares the thermal conductivity of 100 nm and 200 nm alumina films.
Our measured thermal conductivity of alumina in the second round of measurement agrees very well within the error bars in the full range of temperature. We observe that with a correct background subtraction measured $k_{alumina}$ is significantly improved and agrees well with literature value[84].

4.7 Conclusion and Discussion

In this chapter, I presented our results of several experiments to explore the effect of long wavelength phonon diffuse surface scattering on the thermal conductance in our micromachined 500 nm thick Si-N bridges. Our results clearly indicate that even in this high temperature range the diffuse phonon scattering causes a decrease in thermal conductance of Si-N bridge. We observed decrease as small as 2% and as large as 18%. The sensitivity of our measurements enables us to determine these small changes. The error in our thermal conductance measurement is less than 1% throughout the temperature range. The change in measured thermal conductance was observed in the temperature range of 77 to 150 K in some cases and in full temperature range (77-325 K) in many cases. The decrease in thermal conductance was also observed as a function of time which could be because of the oxidation or hydrogenation of Si-N surface which could be a cause of introducing surface roughness. The discovery of long wavelength phonon diffuse scattering in this temperature range presents more challenges in the thermal conductivity measurements of thin films (especially low thermal conductivity thin films). Although the method (described in previous section) of series of deposition of films on the same bridge seemed to reduce the errors in thermal conductivity measurements which is caused by the diffuse surface scattering in Si-N bridges. The value at which the thermal conductance becomes saturated is still an open question which we expect to investigate next. The saturated value of thermal conductance would be different for different
thicknesses and dimension of Si-N membrane because the thermal conductance is a geometry dependent physical quantity and diffuse phonon surface scattering has also shown geometrical dependence at low temperatures[61]. Thus, performing similar experiments on different thickness of Si-N bridges would help answering these question. Our results show that long wavelength phonons diffuse surface scattering does play a role in altering the thermal conductance through Si-N in this relatively high temperature range of 77-325 K.
Chapter 5

Measurement of thermoelectric properties of \textit{a}-silicon metal alloy films

5.1 Introduction

Amorphous materials do not possess long range order. These materials have distinct electrical and thermal transport properties which have been studied for several years and are still under investigation. When silicon is grown as thin film by vapor deposition, it takes the amorphous structural form. The covalent bonds in crystalline silicon (\textit{c}-Si) break to produce dangling bonds as a result of no long range order in amorphous silicon. The presence of these dangling bonds in amorphous silicon (\textit{a}-Si) change its electrical and thermal properties drastically as compared to \textit{c}-Si. Amorphous silicon can only be grown as thin films on small as well as on large areas. There are several applications of amorphous silicon in thin film technology. It is used in the thin film transistors as an active layer which are used in LCD screens.
Figure 5.1: Left: Two 250 x 250\(\mu\text{m}^2\) islands connected to the Si frame through eight legs with Mo heaters & thermometers patterned on each and also connected together by a 806\(\mu\text{m}\) long, 35\(\mu\text{m}\) wide & 500nm thick Si-N suspended bridge. Middle: The similar device patterned with two metal (Mo) triangular leads on each island for thermopower measurement. Right: Closer look of one of the island with leads to measure thermopower.

It is also used as an insulating layer in superconducting integrated circuits[85].

Amorphous silicon alloy is an interesting system to investigate from technological point of view and for fundamental physics applications. This system has been studied for various types of impurities. For example, spontaneous anisotropy of resistivity in \(a\)-Si-Fe[86], metal insulator transition and magnetoresistance in \(a\)-Si-rare earth metal alloys[87, 88], electrical and optical properties in \(a\)-Si-Ni alloy films[89], and thermopower and electronic properties in \(a\)-Si-Ga[90] and \(a\)-Si-Al[91] alloys. Despite all these studies and more, there is very less to no conclusive data available for describing thermoelectric behavior and figure of merit for \(a\)-Si alloy thin films.

In this chapter, I will discuss the preparation of \(a\)-Si metal alloy films and measurement of thermal conductivity, electrical conductivity and thermopower in these films as a function of temperature. Our technique of measuring absolute thermopower in thin films will also be discussed.
Figure 5.2: *Left:* The sample mount with several different pockets for the chip and Si-N substrates to be glued with silver paint. *Middle:* Chip with thermal isolation platforms is silver painted in the center square. *Right:* Shadow mask covers the platform but exposes the Si-N bridge and lead to evaporating material through a small square (which is not visible in this image).

Figure 5.3: (a) Side view: when the shadow mask is being aligned on the platform, (b) Top view: after shadow mask is aligned on the platform for symmetrical deposition of the film on both leads and on Si-N bridge.
5.2 Experimental technique

5.2.1 Thermal Isolation platforms

Our micromachined thermal isolation platforms which we have used to measure in plane thermal conductivity of Si-N membranes [79] are modified to do thermopower measurements in thin films[92] in addition to in plane thermal conductivity measurements. Figure 5.1(a) shows the SEM micrograph of our thermal isolation platform for in plane thermal conductivity measurement. In Figure 5.1(b) triangular metal leads are visible which are added to the platforms in order for the film to make good electrical contact on both ends (hot and cold) of the film, when deposited. So that the voltage generated due to temperature difference can also be measured in addition to the thermal conductivity (See Figure 5.1c). The reason of these leads to be triangular in shape will be discussed later in this chapter.

5.2.2 Preparation of a-Si and its Alloys

We prepared our samples of amorphous silicon by e-beam evaporation and amorphous silicon metal alloys by co-deposition. We have studied two Si-alloy thin film systems, (i) Si-Cu and (ii) Si-Al. In the preparation of the sample films silicon was e-beam evaporated while the copper (or aluminum) was simultaneously thermally evaporated in ultra high vacuum chamber (UHV) on the Si-N bridge shown in Figure 5.1b. In order for the film to be deposited on the bridge as well as symmetrically on the triangular leads on both sides, a silicon shadow mask is designed. This mask covers the whole platform and exposes only the Si-N bridge and the leads to the evaporating material (see Figure 5.3b). The thermal isolation platform is micromachined on a 1x1 cm$^2$ Si wafer. In order to prepare the platform for film deposition, this 1x1 cm$^2$ chip is glued on the sample mount using silver paint and the shadow mask is carefully aligned on the chip under an optical microscope (See Figure 5.2.1).
The shadow mask is held in place with four screws at the corners.

After alignment the platform looks as shown in Figure 5.3 (a) & (b) from two different views. These triangular leads prevent the film to fall on patterned heaters and thermometer in case the alignment is not 100% and hence prevents any shorts between heaters and thermometers. The other advantage of these wide leads is, in case of the source material and the sample mount is not a same z-axis, it prevents any shadowing of the lead area through the mask edges.

5.2.3 Thermal conductivity, Thermopower, & Electrical conductivity measurements

The experimental technique of measuring thermal conductivity is described elsewhere[79] as well as in previous chapters. The new modified platform, shown in Figure 5.1 (b) and (c), enables us to do thermopower ($\alpha$) and electrical conductivity ($\sigma$) measurements on the deposited film in addition to thermal conductivity ($k$) measurement. Making all measurements on one sample eliminates any uncertainty which comes from geometry, composition and handling of the sample. This technique enables us to directly calculate the Figure of merit ($ZT$) as a function of temperature using measured physical properties ($k$, $\sigma$, $\alpha$). Figure 7.1 shows thermal model of our technique which represents our micromachined thermal isolation platform. In order to measure thermoelectric power measurement, a temperature difference ($\Delta T$) is established between two ends of the deposited film by applying current to the heater on one of the islands and thermally generated voltage ($\Delta V$) is measured across the film. We then gradually increase the temperature difference by increasing power and measure voltage at every $\Delta T$. Therefore, the thermopower at each reference temperature comes from the slope of $\Delta V$ versus $\Delta T$ curve and is given as,

$$\alpha = \frac{\Delta V}{\Delta T} \quad (5.2.1)$$
Figure 5.4: (a) Thermal model representing our micromachined thermal isolation platform. (b) SEM micrograph of the platform showing two Si-N islands suspended over Si etch pit and are fabricated with heater and thermometers. A thermometer on the frame is also visible on the top right corner of the image.
The triangular leads on the two sides along the Si-N bridge are also used to measure the resistance of the deposited film. The resistance is then converted into resistivity, \( \rho \), using the dimensions of the Si-N bridge and the thickness of the deposited film and hence converted into electrical conductivity \( (\sigma = 1/\rho) \).

5.3 Results

5.3.1 Electrical Conductivity of Si-Cu and Si Al alloy thin films

The electrical resistivity of undoped, pure amorphous silicon is very high[94]. One application of \( a \)-Si is its use as insulating layers in superconducting devices[85]. As stated earlier, amorphous silicon (\( a \)-Si) carries a high degree of disorder in its structure and as result has a high concentration of dangling bonds. This bonding structure is responsible for the electronic properties in \( a \)-Si. The disorder in \( a \)-Si causes band tails near conduction and valence bands (see Figure 5.5). These tails are often called localized states because they lie below the mobility edge and are
Table 5.1: RT Electrical Conductivity of Si\(_{(1-x)}\)Cu\(_x\)

<table>
<thead>
<tr>
<th>Thickness (nm)</th>
<th>(~\text{Cu/Si at.ratio}\times^*)</th>
<th>Resistivity ((\Omega\text{cm}))</th>
<th>Conductivity ((\Omega\text{cm})^{-1}))</th>
<th>Growth Pressure (Torr)</th>
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<tr>
<td>100</td>
<td>0.1</td>
<td>0.243</td>
<td>4.1</td>
<td>(10^{-8})</td>
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<tr>
<td>100</td>
<td>0.2</td>
<td>0.158</td>
<td>6.3</td>
<td>(10^{-7})</td>
</tr>
<tr>
<td>92</td>
<td>0.25</td>
<td>(9.48\times10^{-3})</td>
<td>105</td>
<td>(10^{-5} - 10^{-7})</td>
</tr>
<tr>
<td>98</td>
<td>0.34</td>
<td>(1.80\times10^{-3})</td>
<td>555</td>
<td>(10^{-7})</td>
</tr>
<tr>
<td>90</td>
<td>0.34</td>
<td>(2.02\times10^{-3})</td>
<td>495</td>
<td>(10^{-7})</td>
</tr>
</tbody>
</table>

*at. ratio is pending confirmation

also referred as trap sites for charge carries. Electrons (or holes) in these states can only contribute to conduction through ‘hopping mechanism’\[95\] by gaining thermal energy at a finite temperature. In pure amorphous silicon, at absolute zero Fermi level lies in the defect states which means no conduction. For a better thermoelectric performance in an amorphous silicon thin film, we improve its electrical conductivity by alloying it with another material which can accept or donate an electron. Alloying shifts the Fermi level towards the valence or conduction band in the localized states near mobility edge (shown in Figure 5.5) which decreases the electrical resistivity in \(a\)-Si and consequently increase electrical conductivity.

We first co-deposited several Si-Cu films of various thicknesses with different atomic percent of Cu on Si-N coated substrates. Room temperature (RT) electrical resistivity of these films were measured using Van der Pauw resistivity technique\[96\]. The results are summarized in table 5.1. For good thermoelectric materials, electrical conductivity is usually desirable which is not \(\gg\) greater than the minimum metallic electrical conductivity value\[97\]. This is because if the electrical conductivity approaches the metallic value it means that the Fermi level has pass through into the conduction band or very close to the mobility edge which is not desirable for better thermoelectric performance. In table 5.1 we see that the electrical conductivity in the Si-Cu films goes up with the atomic percent of copper, as expected. Figure 5.6 shows a plot of electrical conductivity as a function of copper concentration in \(a\)-Si.
Figure 5.6: Measured room temperature electrical conductivity of Si-Cu alloys films as a function of atomic ratio of Cu.

Table 5.2: Three Si$_{(1-x)}$Cu$_x$ thin film deposited on Si-N bridges

<table>
<thead>
<tr>
<th>Sample #</th>
<th>t (nm)</th>
<th>Si rate (A/sec)</th>
<th>Cu rate (A/sec)</th>
<th>Cu/Si at.x</th>
<th>RT $\rho$ ($\Omega$ cm)</th>
<th>RT $\sigma$ ($\Omega$ cm)$^{-1}$</th>
<th>Growth P (Torr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>609</td>
<td>1.5</td>
<td>0.1</td>
<td>$\sim$0.11</td>
<td>23.4x10$^{-3}$</td>
<td>42.7</td>
<td>6.9x10$^{-7}$</td>
</tr>
<tr>
<td>2</td>
<td>265</td>
<td>1.8</td>
<td>0.1</td>
<td>$\sim$0.15</td>
<td>13.6x10$^{-3}$</td>
<td>73.3</td>
<td>1.0x10$^{-7}$</td>
</tr>
<tr>
<td>3</td>
<td>146</td>
<td>2.5</td>
<td>0.1</td>
<td>$\sim$0.07</td>
<td>43.8x10$^{-3}$</td>
<td>22.7</td>
<td>10$^{-7}$</td>
</tr>
</tbody>
</table>

* at. ratio is pending confirmation

There is some uncertainty in the measured electrical resistivity due to the thickness variation of the film caused by rate fluctuations. The composition of the films could also be slightly different because of the same reason. The highest electrical conductivity in the Si-Cu films was achieved for 34 atomic % of Cu.

The electrical conductivity of semiconductor alloys decrease exponentially as a function of temperature which is mathematically represented as

$$
\sigma = \sigma_0 exp\left(\frac{-|E_m - E_F|}{k_BT}\right)
$$

(5.3.1)
Table 5.3: Two Si\(_{1-x}\)Al\(_x\) thin film deposited on Si-N bridges

<table>
<thead>
<tr>
<th>Sample #</th>
<th>t (nm)</th>
<th>Si rate (A/sec)</th>
<th>Al/Si (x^\ast)</th>
<th>RT (\rho) ((\Omega\text{cm}))</th>
<th>RT (\sigma) ((\Omega\text{cm})^{-1})</th>
<th>Growth P (Torr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(\sim100)</td>
<td>1.1</td>
<td>Low</td>
<td>(434\times10^{-3})</td>
<td>2.3</td>
<td>(1.3\times10^{-7})</td>
</tr>
<tr>
<td>2</td>
<td>(\sim100)</td>
<td>0.7</td>
<td>High</td>
<td>(75\times10^{-3})</td>
<td>13.3</td>
<td>(1.4\times10^{-7})</td>
</tr>
</tbody>
</table>

\(\ast\) at. ratio is pending confirmation due to Al rate monitoring issues

Figure 5.7: Measured electrical conductivity of Si-Cu and Si-Al thin films as a function of temperature compared with Si-Y and Si-Gd alloys[87].
where $\sigma_o$ is the temperature independent electrical conductivity, $E_m$ ($E_v$ for holes and $E_c$ for electrons) is the energy at the mobility edge, $E_F$ is the Fermi energy, $k_B$ is the Boltzmann constant, and $T$ is the absolute temperature. Measured electrical conductivity in our samples obeys equation 5.3.1.

### 5.3.2 Thermopower of Si-Cu and Si-Al thin films

The thermopower of the Si-Cu and Si-Al films were measured as a function of temperature. A series of powers were applied on one side of the film (on one island) to establish a temperature difference at the two ends of the deposited film at a given reference temperature. The heating on one side causes a temperature difference of 0.15 K to 20 K for the range of applied powers and thermally generated voltage, $\Delta V$, is measured across the film at each temperature difference, $\Delta T$. The slope of the temperature difference versus thermoelectric voltage gives thermopower at each reference temperature. An example of $\Delta T$ vs $\Delta V$ is shown in Figure 5.8a.

According to Dandee Model[98] which explains transport mechanism in doped amorphous silicon, thermopower in the middle and low, below Debye temperature regime obeys the following equation,

$$\alpha = \frac{k_B}{e} \left( -\frac{(E_m - E_F)}{k_B T} + A \right)$$  \hspace{1cm} (5.3.2)

where $E_m$ ($E_v$ for holes and $E_c$ for electrons) is the energy at the mobility edge, $E_F$ is the Fermi energy, $k_B$ is the Boltzmann constant, $A$ is the heat transport term which is $\sim 1[99]$, and $T$ is the absolute temperature. Figure 5.8b shows measured thermopower of two Si-Cu films. The Cu atomic percent in these two films is very similar which gives similar thermopower. The magnitude of the thermopower is small. It is clear from the equation 5.3.2 that thermopower is linearly dependent on $(E_m-E_F)$. Doping of $a$-Si with a metal changes the $E_F$ and hence changes the $E_m$. 

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A higher metal concentration would move the Fermi level towards the mobility edge causing a decrease in thermopower. The third Si-Cu film with lower concentration of Cu (~7\%) had a very high electrical resistance (bad electrical contact) for thermopower measurements.

Figure 5.9 shows measured thermopower of two Si-Al films with two very different Al concentration. The top curve in the Figure 5.9 is for the Si-Al film with low Al concentration which gives a higher thermopower and the bottom curve is for the film with high Al content. The thermopower is reduced by two orders of magnitude for the increases Al content. Measured thermopower in both Si-Al films starts as negative at 77 K and becomes positive around 160 K. This behavior suggests dual charge carrier transport in our samples and can be explained using multiple carrier transport model which has been used to explain thermopower in other silicon alloy systems[100, 101].

When the thermopower in our Si-Al films is negative and large for lower temperatures, the transport is dominated by electrons near defect states. When the thermal energy of the system is increased by increasing temperature, the contribution to the thermopower dominated by holes from the impurity atoms near mobility edge. This results in a positive and small thermopower at higher temperatures.

In Figure 5.10, measured thermopower of Si-Al film with small atomic percent of aluminum is compared with thermopower of rough silicon nanowires and also with high temperature data available for relatively very thick hydrogenated Si-Al alloy. Our measured thermopower is similar in magnitude at low temperature when compared with rough silicon nanowire[5] and agrees very well in the high temperature limit with sputtered H:Si-Al alloy data[91].
Figure 5.8: a) A linear plot of $\Delta V$ vs $\Delta T$ showing the slope (thermopower) at $T=275$ K our Si-Cu film, b) Measured thermopower of Si-Cu films as a function of inverse temperature, (inset): A general behavior of thermopower for p and n type semiconductor as a function of inverse temperature[90].
Figure 5.9: Measured thermopower of Si-Al 100 nm thick films as a function of inverse temperature. The top curve is for a sample with low Al content and the bottom curve shows for high Al content in silicon.

Figure 5.10: Measured thermopower of Si-Al film with low Al content is compared with the thermopower of 48 nm rough silicon nanowires[5] and sputtered H:Si-Al alloy data[91] a function of temperature.
5.3.3 Thermal conductivity of Si-Cu and Si-Al alloy thin films

Thermal conductivity is an important physical property in general and especially in the search of a good thermoelectric material as described in the first chapter. Amorphous silicon (a-Si) has low thermal conductivity due to the lack of long range order. Heat transport in a-Si is governed by phonons. When we add impurity in a-Si to increase the density of charge carriers we also provide more scattering centers to the phonons which further reduces the thermal conductivity.

Figure 5.11a & b show measured thermal conductance and the background subtraction for two Si-Cu films of thicknesses 609 nm and 265 nm respectively. The copper concentration in these two films are ∼ 11% and ∼ 15%Cu, respectively. These Si-alloy films are low thermal conductivity films and we see a small contribution to the total thermal conductance in both cases. A relatively thicker film (see Figure 5.11) shows a good contribution to the background thermal conductance and hence reduces the error subtraction error. It is important to specify here that the possible reduction in the background due to the increase in surface roughness (which has been discussed in previous chapter) may also be the dominating cause of error but it has been taken into account in the error calculations.

Figure 7.2 shows measured thermal conductance and background subtraction for Si-Al film of thickness ∼ 100 nm with a small (less than 5%) atomic percent of Al. Since these are low thermal conductivity films, large error in thermal conductance of the measured film comes from the subtraction. This error can be reduced by growing thicker films or fabricating our thermal isolation platforms with thinner Si-N membranes. The smaller contribution to the thermal conductance of these alloy films with in the error bars also suggests that adding impurity in the a-Si films reduces the thermal conductivity as expected. Thermal conductivity of these films were calculated using measured thermal conductance (K) and the geometry
Figure 5.11: a) Measured thermal conductance and the background subtraction for Sample 1: a 609 nm thick Si-Cu alloy film with \(\sim 0.11\) at. % of Cu, b) Measured thermal conductance and the background subtraction for Sample 2: a 265 nm thick Si-Cu alloy film with \(\sim 0.15\) at. % of Cu.
Figure 5.12: a) Measured thermal conductance and the background substation for Si-Al film of \( \sim 100 \) nm thick with low concentration of Al.

of the bridge by using \( k = Kl/wt \), where \( w \) and \( l \) are the length and width of Si-N bridge and \( t \) is the thickness of deposited film. Figure 7.3 compares measured thermal conductivity of Si-Cu and Si-Al alloy films with the thermal conductivity of pure \( a-Si[102] \) and with thermal conductivity of silicon nanowires reported by two groups\([5, 40]\). Our measured thermal conductivity of both silicon metal alloy films of different thickness and atomic percent of the added impurity is lower than the pure amorphous Si, as expected. The addition of impurity causes reduction in thermal conductivity as compared to pure \( a-Si \). Thermal conductivity of our two silicon alloy thin film is also lower than the reported thermal conductivity of silicon nanowires.

5.4 Conclusion

In this chapter, I presented our results of measurement of thermal conductivity (\( k \)), thermopower (\( \alpha \)) and electrical conductivity (\( \sigma \)) of Si-Cu and Si-Al alloy films of different thicknesses with various atomic percent of impurity atoms (Cu and Al). Our results of thermal conductivity and electrical conductivity measurement show that
Figure 5.13: Comparison of the measured thermal conductivity 609 nm (≈11% Cu) and 265 nm (≈15% Cu) thick Si-Cu films and 100 nm (<5% Al) Si-Al alloy films with 270 nm a-Si[102], 50 nm SiNW[5] and 20 nm[40].

when we add impurity in amorphous silicon thermal conductivity reduces but is not very much affected by the nature and concentration of the impurity. The reduction of the thermal conductivity is the key in search of potentially better amorphous silicon based thermoelectric thin films. Our electrical conductivity measurements show that for similar atomic concentration of a metal we get similar electrical conductivity values which is roughly independent of the type of impurity atom. The thermopower measurement results show that thermopower in these alloy is very sensitive to the atomic percent and to the nature of added impurity. For optimized thermopower, low concentration of impurity gives better results. If we tune the concentration level of the impurity we can find an optimized point where a combination of thermopower, electrical conductivity and thermal conductivity can give an enhanced ZT at a given temperature. Our technique of measuring these properties (thermal conductivity ($k$), thermopower ($\alpha$) and electrical conductivity ($\sigma$)) enables us to directly measure the Figure of Merit for thin films on one sample in a wide
temperature range of temperature. This eliminates any errors which come from geometrical and compositional variance in the sample. Overall, amorphous silicon alloy thin film system has a great potential to be studied in search for potentially better, easy to prepare thermoelectric films.
Chapter 6

Comparison of Thermometer Calibration

6.1 Introduction

In all of our measurements of thermal conductivity, thermopower and electrical conductivity we measure temperature by measuring the resistances of the thermometer on frame and on each island. All the thermometers which are discussed in this chapter are made of the metal, molybdenum (Mo). We then calibrate these thermometers for temperatures. This is a standard way to measure temperature on small scale. This is also called resistance thermometry. In this chapter, I will compare the calibration (which is R vs T relation) for measurements which has been done on a same chip several times as in different cryostat and at different excitation voltage.
6.2 Resistance measurement

6.2.1 Four wire resistance measurement

In a four wire resistance measurement, current is applied through the resistor using two leads and voltage drop across the resistance is measured using other two leads unlike a standard multimeter. So that only the resistance of the sample resistor is measured and no lead resistance will cause an error in the measured value. Another way to do it is to apply potential difference (which will be called excitation voltage in rest of the chapter) across the resistor and measure the current through it to calculate the resistance using Ohms’s low, \( V=IR \). All of our resistance measurements are done using four wire measurement technique so that thermometers are calibrated properly.

6.2.2 Sensitivity of a thermometer

In resistance thermometry, sensitivity of a thermometer is calculated by the slope of \( R \) vs \( T \) plot. The slope \( (dR/dT) \) tells us that how a resistor response to the change in temperature. A higher slope means a big resistance change in a small change in temperature which is usually desirable in a good sensitive thermometer. From this slope, absolute sensitivity can be calculated as,

\[
S = \left( \frac{dR}{dT} \right) \left( \frac{T}{R} \right)
\]  

(6.2.1)

A good thermometer has a sensitivity of 0.1 and higher[103].

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6.3 Comparison of calibration as a function of excitation voltage

On each thermal isolation platform there are three thermometers. In this section I will compare thermometer’s calibration and sensitivity as a function of excitation voltage. This measurement was done in the low temperature Helium-3 cryostat. Figure 6.1a compares a resistance vs temperature plot of the thermometer on one of the islands on the same chip measured with two different excitation voltages (1 & 3 mV). The inset of figure shows the zoomed viewed so that the comparison becomes visible. We see that there is not much difference in the resistance but the sensitivity of the thermometer is improved (shown in figure 6.1b) for 3 mV excitation. This is because an improved slope (shown as inset in 6.1b) of the resistance vs. T plot. A higher excitation voltage gives a better signal to noise ratio which improves the sensitivity of the thermometer. It is important that we do not increase excitation voltage high enough to cause self heating of the thermometer. The self heating is indicated by the fact that the resistance of the thermometer starts increasing at a constant temperature and the resistor do not show Ohmic behavior.

6.4 Comparison of calibration measured in two different cryostats

This section compares the thermometer calibration and sensitivities of a thermometer measured on a same chip measured in two different cryostats at different times. Figure 6.2a shows the R vs T plot for the thermometer on one of the island. The resistance is very slightly different (~ 0.1 Ω) but the slope of R vs T plot (see inset of figure 6.2b) measured in Liquid Nitrogen cryostat is slightly noisier than the one measured in Liquid Helium cryostat (Liquid nitrogen was used for cool down).
Figure 6.1: a) Compares the calibration of a thermometer measured at two different excitation voltages, (inset) shows a zoomed in view of the calibration curve, b) Sensitivity of the thermometer plotted as function of temperature for 1 and 3 mV excitation, (inset) shows the slope of the calibration plot.
There could be several reasons of the noise, a lose wire, a bad connection, improper grounding or noise coming from bad temperature regulation. Therefore, the thermometer sensitivity which is defined by the slope becomes noisy which is shown in figure 6.2b. The reasons of noise mentioned above should be inspected if a greater noise is seen in thermometer sensitivity. A careful increase in the excitation voltage could also help improving the sensitivity.

6.5 Comparison of calibration on different temperature steps (ΔT)

In this section the calibration of the thermometers is compared when calibrated at different temperature steps. Figure 6.3a shows the resistance versus temperature plot for calibration at every 2 K and every 4 K temperature step. The difference in resistance in these two calibration at one temperature value is ∼ 5 Ω which is about 0.3 % of the value calibrated at ΔT=2 K. The slope and sensitivity of the thermometer are better in both measurements and are not much affected by the temperature calibration steps as shown in figure 6.3b and its inset.

6.6 Comparison of calibration measured at different times

In this section, I will compare thermometer calibration when it is measured more than once at different times. There are several platforms which we have measured many times but here I am giving an example of two chips (C1LL and A3LL) which has been mentioned in previous chapters. Figure 6.4a shows the comparison of resistance of the thermometer on one of the islands measured at four different times. In the inset of 6.4a which is the zoomed view of the calibration curve, it is clearly seen that the resistance measured fourth time is about 3 to 4 Ohms different from
Figure 6.2: a) Compares thermometer calibration measured in two different cryostats, (inset) shows a zoomed in view of the calibration curve, b) Sensitivity of the thermometer plotted as function of temperature measured in LN$_2$ and He-3 cryostat, (inset) shows the slope of the calibration plot.
Figure 6.3: a) Compares thermometer calibration measured at every 2 and every 4 K, (inset) shows a zoomed in view of the calibration curve, b) Sensitivity of the thermometer plotted as function of temperature measured at $\Delta T = 2$ and 4 K, (inset) shows the slope of the calibration plot.
the initial value. Although there is not much change in sensitivity and slope of the R vs. T plot when compared in all the measurements. It is shown in figure 6.4b and its inset. The thermometer shown in 6.4a is the thermometer on the heated island. In order to make sure that this slight off set in resistance is not due to heating, I plotted thermometer on the frame (R1) which is shown in figure 6.5 and a shift in resistance is visible in the inset of figure 6.5. So over a period of more than two months and after several measurements, we observe a small change in the resistance of all three thermometers on the chip. This could be because of oxidation of the metal with which these thermometers fabricated. In a similar comparison for an other chip (A3LL), frame thermometer is compared in four measurement made at different times. Figure 6.5a and b shows the calibration curve and the sensitivity of the thermometer. The inset of 6.5b shows the slope of calibration curve. A shift in the resistance is seen in the fourth measurement of the resistance.
Figure 6.4: a) Compares thermometer calibration measured at four different times, (inset) shows a zoomed in view of the calibration curve where a slight shift in resistance is visible, b) Sensitivity of the thermometer plotted as function of temperature, (inset) shows the slope of the calibration plot.
Figure 6.5: Compares frame thermometer calibration measured at four different times, (inset) shows a zoomed in view of the calibration curve where a slight shift in resistance is visible.
Figure 6.6: a) Compares thermometer calibration measured at four different times, \textit{(inset)} shows a zoomed in view of the calibration curve where a slight shift in resistance is visible, b) Sensitivity of the thermometer plotted as function of temperature, \textit{(inset)} shows the slope of the calibration plot.
6.7 Summary & Conclusion

The comparison of calibrations in different situations shows that in some cases we see small changes in resistances. The calibration at small steps of temperature is more accurate than bigger temperature steps. A proper excitation voltage which does not cause self heating can improve the sensitivity of the thermometer and reduce the noise. Other factors that can affect the thermometer sensitivity and improve the measurement quality are the proper connections and grounding. In conclusion, it is important to calibrate thermometers every time we measure a chip, even though it has been calibrated before. The assumption that the calibration would same in all situation could cause error in the measurements.
Chapter 7

Electron beam Lithography & Nanostructuring

7.1 Introduction

Electron beam lithography is a technique which is widely used to pattern nanoscale structures for scientific research, fundamental physics, and advanced technological and industrial applications. The instrument that is used for e-beam lithography is called the Scanning Electron Microscope (SEM). This chapter provides information about e-beam lithography and our efforts to scale down the thermal isolation platforms described in chapter 2 & 3. I will also discuss a few new techniques of patterning nanowires on suspended Si-N bridges[79].

7.2 What is e-beam lithography?

Electron beam lithography as indicated by its name is when an electron beam makes desired patterns on a sample or a substrate. The substrate can be a bare silicon (Si) wafer or coated with a material or any other surface where patterns are desired to
be generated. E beam lithography is a multi step process. The standard steps for ebeam lithography are as follows:

1. Coating sample with a resist
2. Baking of resist
3. Exposure to electron beam
4. Developing of sample after exposure
5. Deposition of desired material on exposed area
6. Removing deposited material from unexposed areas called liftoff process

7.2.1 Preparing the sample: PMMA Coating

To prepare our sample for lithography, we first coat it with a polymer called Poly Methyl Methacrylate (PMMA). It is the synthetic polymer of methyl methacrylate. It is basically a solution consisting of the polymer in a solvent and is used to spin coat the sample where lithography needs to be done. PMMA works as a resist in the electron beam lithography process. Spreading PMMA on substrate is done using a spinner shown in Figure 7.1b. With spinner, a substrate is held by a vacuum, we then program the spinner so that the sample rotates at a certain speed with a specific acceleration for a desired amount of time. Once PMMA is dispensed onto it, these parameters (speed, time, and acceleration) decide the thickness of PMMA onto sample. PMMA can be dispensed on a sample using standard methods[104].

7.2.2 Baking of sample

When the sample is coated with PMMA, it needs to be baked at a certain temperature (usually 100°C or 170°C for 30 or 60 mins, respectively) to evaporate the residual solvents. Now the substrate or the sample is ready for lithography.
7.3 Exposure to electron beam

A scanning electron microscope is used for exposing the sample to electron beam. Patterns can be made by an electron beam, deep UV light or X-rays. Exposure of the sample to the beam breaks the chain bonding structure within PMMA. This process is usually referred as de-cross linking. With PMMA resist very fine (nanoscale) channels can be generated. The process of exposure is followed by developing the sample in MIBK/IPA (1/3) developer for 70 seconds followed by 20 seconds in Isopropanol. This Developer consists of Isopropyl alcohol, Methyl isobutyl ketone.

The microscope used for the lithography described in this chapter is JOEL JSM IC848A (shown in Figure 7.1a). More details about this microscope can be found elsewhere[105].

7.3.1 Optimization and focusing the beam

After properly loading and transferring the sample in the SEM specimen chamber, beam optimization is the first and important thing for writing fine, high resolution patterns. Optimization is usually done at a beam current which will be used to write the patterns. A slight difference in the optimization current and the writing current (usually specified in an Nano Pattern Generation System-NPGS run file) could result into over or under dosing of the sample. Beam current is measured
Figure 7.2: SEM Micrograph of a Faraday Cup, a metal (Cu) round shape disc which is glued down to the sample mount using carbon tape. There is a hole in the center where the beam is focused to measure beam current.

When the beam is focused in the Faraday cup. A Faraday cup collects the charged particles in a vacuum. It consists of a conductive metal with a hole (See Figure 7.2). By measuring the number of charged particles hitting the cup, the resulting current can be measured [106]. Mathematically, it is expressed as $I = \frac{Nq}{t}$, where $I$ is the measured current, $\frac{N}{t}$ is the number of charged particles hitting the Faraday cup per unit time and ’$q$’ is the charge on an electron ($1.6 \times 10^{-19}$ C).

To begin optimization, the beam is moved to and focused on a gold (Au) coated substrate (commonly referred as Au standard) which is used to optimize beam. When the beam hits the surface of Au standard, a slight decrease in the beam current is observed. This is due to the scattering of electrons from the Au surface and ammeter measures a reduced flux of emitting electrons. This does not effect the optimization and lithography and is perfectly normal to observe. When the beam is well focused and optimized on the Au standard, the Au particles look round and clear, as shown in Figure 7.3. The particles in Figure 7.3 look blurry but this is due to the presence of noise when a digital image is taken at a very high resolution.
7.4 Lithography on suspended Si-N membrane

Lithography on the a plane Si or Si-N coated substrate is a straightforward process. In order to generate patterns using e-beam lithography on a suspended Si-N structure, we need to adopt different strategies for getting a uniformly spreaded PMMA on the suspended structure. The tricky part is to avoid getting PMMA under the suspended structure (into the etch pit). The reason is that during baking, PMMA shrinks and causes an inward stress on the suspended structure which could break it.

7.4.1 Spraying PMMA using an airbrush on Si Substrates

An airbrush (see Figure 7.1c) is used with clean nitrogen gas to spray PMMA on the sample while it was spinning at a constant speed. Since it was a non-standard method of getting PMMA on a sample, the first task was to find out that is it possible to coat the sample with a uniform layer of PMMA using this spraying technique? The coating of a substrate is one of the most important aspect of successful e-beam lithography. Before trying air brushing PMMA on a suspended structure, I tested
this technique on bare Si substrates for various spin speeds, time for spraying, and time of spin. I performed several iterations of these parameters. Few of those trials were successful and few were not. I summarize the first iteration in table 7.1 where the spin speed was changed while the time of spraying remained constant. [NOTE: It is important to clean the airbrush with acetone and isopropanol everytime it is used for spraying PMMA to prevent the fine nozzle of brush from blocking with PMMA residue].

Though the thickness of PMMA on these substrates were unknown but the idea was to go through all the lithography steps and see which one of these substrates give good high resolution lithography. If the PMMA surface looks colored before or after the baking (these samples were baked for 30 mins at 170 °C), it suggests a varying thickness of PMMA or non uniformity in the thickness. It is possible that the PMMA on the sample looks uniform before and non uniform after the baking. The samples which showed color contrast were not used for lithography. Unfortunately, in all of the above cases, the only sample which looked reasonable after baking was the one which was spun at the speed of 3000 rpm while PMMA was sprayed for 5 sec while it was spinning. A standard test lithography pattern was

<table>
<thead>
<tr>
<th>Sample No.</th>
<th>Spin Speed (rpm)</th>
<th>Total Spin Time (Sec)</th>
<th>Spray Time (Sec)</th>
<th>Spray Condition</th>
<th>Result (pre bake)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>500</td>
<td>45</td>
<td>5</td>
<td>spinning at 500 rpm</td>
<td>uniform spread</td>
</tr>
<tr>
<td>2</td>
<td>1500</td>
<td>45</td>
<td>5</td>
<td>spinning at 500 rpm</td>
<td>uniform spread</td>
</tr>
<tr>
<td>3</td>
<td>20</td>
<td>45</td>
<td>5</td>
<td>spinning at 500 rpm</td>
<td>non uniform spread</td>
</tr>
<tr>
<td>4</td>
<td>3000</td>
<td>45</td>
<td>5</td>
<td>spinning at 500 rpm</td>
<td>uniform Spread</td>
</tr>
<tr>
<td>5</td>
<td>1500</td>
<td>45</td>
<td>5</td>
<td>static</td>
<td>non uniform Spread</td>
</tr>
</tbody>
</table>
written on the sample at a beam current of 25 pA. After developing the sample, gold was sputtered on it for about 25 secs which gives an estimated thickness between 10-20 nm. The sample was imaged before liftoff the fine features can be seen after developing the sample (SEM image shown in Figure 7.4). The liftoff process was not done because Au was not deposited with a sticking layer. For the liftoff process, a sample is soaked in acetone over night to remove metal layer from unexposed areas but in this case, acetone would have removed all metal (Au) from the sample. From this test, I concluded that the spin speed of 3000 rpm for air brushing is good for lithography. Since the liftoff process was not performed on this sample, it was unknown whether this lithography is good enough to produce post liftoff, high resolution nano features. One human error which could cause variation in the results is the distance from which PMMA was sprayed. I tried to be at the same spot every time but this should definitely be considered if results differ for similar spraying conditions.

I picked the 3000 rpm spin speed from this first iteration. In the next iteration
Table 7.2: Iteration 2: PMMA Spin on Si substrate using airbrush

<table>
<thead>
<tr>
<th>Sample No.</th>
<th>Spin Speed (rpm)</th>
<th>Total Spin Time (Sec)</th>
<th>Spray Time (Sec)</th>
<th>Spray Condition</th>
<th>Result (pre bake)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3000</td>
<td>45</td>
<td>5</td>
<td>spinning at 500 rpm</td>
<td>uniform Spread</td>
</tr>
<tr>
<td>2</td>
<td>3000</td>
<td>45</td>
<td>5</td>
<td>spinning at 500 rpm</td>
<td>uniform Spread</td>
</tr>
<tr>
<td>3</td>
<td>3000</td>
<td>45</td>
<td>7</td>
<td>spinning at 500 rpm</td>
<td>non uniform Spread</td>
</tr>
<tr>
<td>4</td>
<td>3000</td>
<td>45</td>
<td>10</td>
<td>spinning at 500 rpm</td>
<td>non uniform Spread</td>
</tr>
<tr>
<td>5</td>
<td>3000</td>
<td>45</td>
<td>10</td>
<td>spinning at 500 rpm</td>
<td>non uniform Spread</td>
</tr>
<tr>
<td>6</td>
<td>3000</td>
<td>45</td>
<td>15</td>
<td>spinning at 500 rpm</td>
<td>uniform Spread</td>
</tr>
<tr>
<td>7</td>
<td>3000</td>
<td>45</td>
<td>15</td>
<td>spinning at 500 rpm</td>
<td>uniform Spread</td>
</tr>
</tbody>
</table>

process of the air brushing PMMA test I changed the time of spraying keeping the spin speed (3000 rpm) and time of spin after spraying (40 secs) constant. The second iteration is summarized in table 7.2.

Sample # 2, 6 and 7 in table 7.2 looked smooth and uniform after baking for 30 mins at 170 °C. I performed lithography on sample# 2 and 6 with a beam current of 25 pA and at a bias voltage of 35 kV. A 50 nm of aluminum (Al) was then thermally evaporated on these samples.

The liftoff process on sample # 2 did not reflect promising results. Metal was lifted off from some areas but not from all. There were no fine features seen after liftoff from which we can conclude that though the PMMA looked uniform before, it might not have been. This is why some areas were over and some were under dosed. When a sample is over dosed it makes the resist negative and it is hard to liftoff the metal around the features. On the other hand if it is under dosed which means that the beam is not making deep channels all the way to the surface of the substrate then we don’t see any features after liftoff.
Figure 7.5: Pre-liftoff images of sample 6 from iteration 2 defined table in 7.2.

Sample # 6 showed better post liftoff results (shown in Figure 7.6). In Figure 7.5, we can see pre-liftoff images of fine features on sample # 6. Figure 7.6 shows post-liftoff images of features on sample # 6. We can see the larger features but not their fine sharp edges. This does reflect a dose problem but probably a beam focus problem which is an essential part of complete optimization process before the sample exposure. If the beam focus is slightly off, the beam spreads out more at the edges and this causes the resulting features as shown in Figure 7.6. Since I had two samples with similar spray conditions, I used sample # 7 from iteration 2 (table 7.2) and repeated the exact same lithography process as was performed on sample # 6. This time extra attention was paid on optimizing the beam. The post liftoff results from this sample (see figures 7.7 & 7.8) show that fine features are visible with sharp edges, there are no metal residues at the edges, and high line width resolution is achieved.

7.4.2 Conclusion & Future Directions: Airbrushing on Si-substrates

The recipe of air brushing for samples 6 and 7 (shown in table 7.2) resulted into successful lithography. The thickness of sprayed PMMA was unknown so I used
Figure 7.6: Post-liftoff images of sample # 6 from iteration 2 defined in table 7.2. *Left* Metal was not completely lifted off to give fine features, *right* Blur edges are seen in a different pattern.

Figure 7.7: Post liftoff images of sample # 7 from Iteration 2 shown in table 7.2. *(Left)*: is the post liftoff image of a test pattern, *(right)*: magnified view of the bottom left pattern in the first image.
Figure 7.8: Post liftoff images of sample # 7 from Iteration 2 shown in table 7.2. (a) Low magnification post liftoff image of lines’ pattern, (b) zoomed in image of lines’ pattern, (c) magnified image of line showing the line width (resolution) of 142 nm.
this spraying recipe on another substrate. The thickness was then measured with profilometry and the result was very close to 1500 Å. This recipe can be used for PMMA coating of samples in addition to standard PMMA spin coating techniques.

### 7.4.3 Spraying PMMA using an airbrush on suspended silicon nitride membrane

The main purpose of introducing the PMMA airbrushing technique on the samples is to be able to use it for lithography on suspended structure as has been discussed in the beginning of section 7.4.

Now we have a successful recipe for air brushing. When we tried this recipe on a suspended structure, we found them broken just after airbrushing and the reason is the pressure with which PMMA comes out from the tip of the airbrush. The pressure was high enough to break the suspended platform in the first few seconds. I then tried two more things: (i) decreasing the pressure in airbrush and (ii) changing the distance from which PMMA is airbrushed. Unfortunately, none of them worked and we ended up with broken structures. The conclusion we can make from these results is that the airbrushing recipe works for plane substrates but not for suspended structures. The recipe defined in table 7.2 needs to be modified for suspended structures since the area of Si-N where we intend to generate patterns is only a few hundred micron square.

The next idea is to sprinkle PMMA (when the sample is static) from a farther distance. This may not give uniformity all over the chip but might give uniform PMMA thickness on micron scale on the platforms. To perform this procedure, the chip was put on a clean surface under the fume hood and sprayed PMMA from a distance of about 12 inches (a foot). In this case, the thickness of PMMA is unknown. The silicon nitride surface I was aiming for is shown with yellow squares in Figure 7.9(a) where as Figure 7.9(b) shows the zoomed in view. I aimed for this
structure because it was a test structure with no metal layer fabricated on it and it was a bare 500 nm thick suspended Si-N structure. The structure shown with red squares in Figure 7.9a has already been patterned with heaters and thermometers using photolithography and this is the platform that we have used for thermal conductivity measurement of Si-N.[79]

Therefore, PMMA was sprinkled using an airbrush at a pressure of 15 psi from a distance of 12 inches for 1 min when the sample was static. Then the sample was baked at 170° C for an hour in the oven. A set of test patterns and a set of lines were written on the suspended membrane with a beam current of 25 pA and accelerating voltage was 35 kV. A 20 nm of Pd with 10 nm of Cr sticking layer was then deposited on the sample after developing. Figure 7.10 shows a test wheel pattern before lift off. We can clearly see that the lines look wider which is caused by the bad z axis focus of the beam. Figure 7.10(b) shows a zoomed view of wheel pattern and Figure 7.10(c) shows a low line width resolution of 271.3 nm because of a bad z focus. So its clear that in a lithography process a slight flaw in optimization can adversely
Figure 7.10: (a) Pre liftoff image of wheel test pattern on suspended Si-N membrane in the first round of lithography. (a) Magnified view of the wheel pattern, (c) highly magnified pre liftoff image of wheel pattern showing a line width of 271.3 nm.

vary the results. Though the lithography in this case is not perfect but it was worth doing a liftoff to check the post liftoff results. Figure 7.11 shows a post liftoff image of the test (wheels) pattern and we see that the metal did not completely liftoff. The same effect was seen in other test patterns on this chip. When we have liftoff problems, there could be more than one reason for it. In this case, the first reason could be non uniformity of the PMMA which we can expect because of the way it was sprinkled. The other reason is when we don’t know the estimated thickness of PMMA we can under or over dose the pattern. Another factor is, even if the PMMA is uniform but not thick enough, it can make the metal liftoff difficult. In this particular case the bad liftoff is dominated by either the fact that PMMA was not spatially uniform or it was so thin that after depositing the metal layer it was hard to remove.
I then tried sprinkling PMMA on another suspended Si-N structure. This time, I sprayed PMMA for about 3 mins from a distance of 12 inches (same as previous) and kept the rest of the lithography and depositing conditions similar. Figure 7.12 and 7.13 show few pre liftoff images with zoomed view and resolution of the test patterns. In Figure 7.12 & 7.13, the line width resolution is improved from the last round and this is because a better optimization.

To study thermal and thermoelectric transport in nanostructures using our micromachined thermal isolation platform (Figure 7.9), we want to develop a technique that enables us to pattern fine nanowires on Si-N bridge. This is why in addition to writing these test patterns I also wrote fine lines on the Si-N legs of the suspended structure shown in Figure 7.9(b). The pre liftoff results of these lines are shown in Figure 7.14. These lines (nanowires) in Figure 7.14(b) do not look continuous which may be because these lines were written with a single estimated dose. The dose may not be sufficient for the thickness of PMMA on the membrane and suggests that channels made with e-beam are not smooth. This sample was soaked in acetone overnight for the metal liftoff process, but the metal was not lifted off on the test pattern and no lines (nanowires) were found after liftoff. This post liftoff result agrees with the pre-liftoff conclusion that the thickness of the PMMA was not
Figure 7.12: (a) Pre liftoff image of a wheel test pattern on suspended Si-N membrane in the second round of lithography. (a) Magnified view of the wheel pattern, (c) highly magnified image of wheel pattern showing a line width of 54.6 nm.
Figure 7.13: (a) Pre liftoff image of DU seal pattern on suspended Si-N membrane in the second round of lithography. (b) Magnified view of pre liftoff image of DU seal test pattern, (c) Highly magnified pre liftoff image of seal test pattern showing a line width of 85 nm.
7.4.4 Conclusion & Future Directions: Spraying PMMA using an airbrush on suspended silicon nitride membrane

In conclusion, the uniform thickness of PMMA is an issue when PMMA is sprinkled because there is a big chance of human error and repeatability. The uniformity of the PMMA thickness is difficult to achieve in this case which can effect the results. Lithography on a suspended structure is possible if PMMA is spun on just the bridge, this requires a way to get PMMA through a very small opening comparable to the size of Si-N bridge. One way to do this is to try spinning PMMA when the whole structure is protected by a shadow mask except the Si-N bridge. This technique is very similar to how we deposit a thin film the Si-N bridge (which is described in chapters 4 & 5). This technique would prevent a large amount of PMMA from falling onto the structure as well as in the etch pit.

7.5 Nanolithography on Si-N bridge

When these (see Figure 7.9) thermal isolation platforms are fabricated, the last fabrication step is the KOH wet etch which etches the silicon to create deep etch pit
and release the islands to be freely suspended over the etch pit. One way to pattern nanowires on the Si-N bridge is to do lithography before the KOH etch. It means that when the islands and the bridge are not suspended but have Silicon substrate underneath. The only problem with this method is that it restricts us to deposit a material for the nanowire which doesn’t etch in KOH etch but it was worth trying.

This time a chip was picked which we use to measure thermopower of thin films because they have metal leads at the both ends of the Si-N bridge so that the deposited film can make good electrical contact (see Figure 7.15). The selected chip has gone through all the fabrication steps except the KOH etch. Then using the standard PMMA spin method, PMMA and CO PMMA (which is a copolymer which is attacked by acetone quicker than the PMMA and makes the lift off process easier) was spun on the sample. In this spin process, 1000 Å of Co-PMMA was spun on the chip and was baked for half an hour at 170° C. Next, a 1500 Å of PMMA was spun and was baked at 170° C for an hour. The aim was to write on the 806 μm Si-N bridge on the thermal isolation platform. The dose for these lines was pre-determined by doing lithography on a bare Si-N substrate. The writing magnification for this pattern was x80. The lines (nanowires) were designed to be long enough to overlap the metal leads at both ends of the bridge. After lithography, a 30 nm Cr layer was thermally evaporated on the chip. Figure 7.16 (a) shows the post liftoff image of the nanowires on the Si-N bridge where Figure 7.16 (b) shows that the Cr nanowires make contact on both sides. Figure 7.16(c) shows the resolution of these wires which is about 373 nm. This resolution is a resealable for the magnification (x80) at which lithography was performed. At this magnification, one would expect a line width resolution of a few hundred nanometers. Seven nanowires were patterned on a 35 μm wide Si-N bridge. The next step in this process is to perform the KOH etch on this chip to release the islands. The other question which arises is whether these wires will survive the process of etching since they are very
Figure 7.15: (a) Optical image of the thermal isolation platform where metal (Mo) leads are visible on both sides of 806 µm Si-N bridge to make an electrical contact with the deposited material on the bridge. (a) magnified view of one of the islands with visible metal lead.

skinny wires.

7.6 Conclusion & Future Directions: Nanolithography on Si-N bridge

This is a technique which can be used to pattern nano structures on the Si-N bridge before it is released and suspended. We can then release the islands & bridge to measure thermopower of these nanowires. The thermal conductivity of these nanowires would have larger error bars due to large contribution to the thermal conductance. In this particular case the thermal conductance of this Si-N bridge was not pre-measured since it was not released. One way to overcome this problem is that after KOH (potassium hydroxide) etch when the islands and the bridge are suspended over the etch pit, perform the measurements of thermopower and thermal conductivity. Once the measurement is completed, etch the Cr wires in Cr etch and then measure the thermal conductance through Si-N bridge. This way we can have both measurements from the bridge (with or without wires). In this case, some errors might come from the variation of Si-N surface while going through multiple
Figure 7.16: (a) Post liftoff SEM micrograph of ebeam lithographically patterned Cr nanowires on the Si-N bridge. (a) Magnified view of the nanowires making contact on the metal lead, (c) highly magnified image of 30 nm thick Cr nanowires on Si-N bridge with a resolution of 373 nm.
chemical processes.

### 7.7 Fabrication of Thermal isolation using e-beam lithography

The thermal isolation platforms (shown in Figure 7.15) are fabricated using standard photolithography. Photolithography is a standard technique for micromachining but when the desirable size of a patterned structure is less than 1 µm then e beam lithography is the technique to use.

These micromachined structures are fabricated using a multistep process (described in chapter 3). The first step is to deposit a metal layer on a Si-N coated substrate and then pattern them in to heaters and thermometers. Alignment marks are an important factor for each fabrication (photo or ebeam lithography) step to go smoothly and to make sure that the patterns are not being written over the previous pattern. Fabricating these platforms with e beam lithography requires lithography steps which need to happen at different times and at different magnifications. To achieve this, I designed (using Express CAD software) a multilayer structure with alignment marks.

In the effort of fabricating reduced size thermal isolation platforms, I did some preliminary fabrication using e-beam lithography. I picked a Si substrate with a 500 nm Si-N deposited on it. I then spun a 1500 Å layer of PMMA onto it and baked it for an hour at 100°C. The structure was intentionally designed at 10 times smaller scale as compared to the thermal isolation platforms shown in Figure 7.15. When a new pattern is designed, the first thing is to determine a proper dose for it. The proper dose is determined by writing a series of patterns with several different doses, this is called an array. The lithography of heaters and thermometer pattern with alignment marks was done on the sample. The sample was then developed and a
30 nm Cr layer was deposited on it. During the liftoff process, the metal layer was patterned into heaters and thermometers as they appear on the islands and shown in Figure 7.17(a). A frame thermometer with its relatively smaller bond pads can be seen in Figure 7.17(b). The zoomed in view of the metal heaters and thermometers is shown in Figure 7.17(c) whereas the line width resolution for this structure is 80 nm which is shown in 7.17(d).
7.7.1 Conclusion & Future Directions: Fabrication of Thermal isolation using e-beam lithography

A first fabrication step of fabricating the thermal isolation platforms at a smaller scale was successfully completed using e-beam lithography. The next step in this process is to spin PMMA on the sample and bake it. The alignment marks from the first fabrication step will then be used to align the sample for the next lithography process. The alignment is a very critical aspect of this multi step lithography. An introduction of the intermediate smaller bond pads would be helpful to guide the measurement leads to the bigger bond pads. The second lithography step does not require a metal layer deposition but a plasma etch. This is to etch windows in the silicon nitride to create pattern of islands and bridge. Finally, a KOH etch needs to be done to release the islands from silicon substrate. A smaller scale silicon nitride based thermal isolation platform would be useful in determining the thermal transport in nanoscale structures and the thermal transport in silicon nitride as a function of sample dimension.
Chapter 8

Conclusion

In this dissertation we have presented the challenges in measuring thermal conductivity in thin films and our efforts to overcome these hurdles. Our micromachined thermal isolation platforms provide a state of the art technique for measuring in plane thermal conductivity in thin films. With the careful design of these platforms we have dramatically reduced main causes of error in thin film thermal conductivity measurements. This silicon nitride (Si-N) based thermal isolation platform enables us to measure thermal conductivity, thermopower and electrical conductivity on a same film thus eliminating uncertainties which arise from composition and geometry of the sample.

Thermal conductance of Si-N was measured and used as a background to the total measured thermal conductance after the film deposition. The results of thermal conductivity measurements of several silicon nitride bridges have been presented. We have also discovered that long wavelength phonon surface (boundary) scattering do play a role in reducing the thermal conductance through silicon nitride bridges when a film is deposited on it. We performed several experiments to verify this behavior. This reduction in thermal conduction presented more challenges for us to measure thermal conductivity in thin films. We then introduced a technique of
depositing a series of various thicknesses of a film which helped in minimizing the error in thermal conductivity measurement caused by surface scattering in Si-N.

In achieving our goal to characterize the thermoelectric performance in amorphous silicon based thin films, we prepared and studied two amorphous silicon metal alloy films. The measurements of thermal conductivity, thermopower and electrical conductivity were conducted for films of various thicknesses and metal concentrations. Our results indicate that thermal conductivity stays low after adding metal in amorphous silicon and electrical conductivity can be predicted for a specific concentration of a metal. Thermopower, on the other hand, is a property which is very sensitive to the nature and concentration of the added impurity. A high thermopower can be achieved for low concentration of metal but the concentration should be tuned for an optimize value of thermopower and electrical conductivity. This is necessary for a better thermoelectric performance in addition to low thermal conductivity of the film. Our results show that amorphous silicon alloy thin films has a potential to be studied for thin films because of their low thermal conductivity and tunable electrical and thermoelectric transport.
Bibliography


[105] Instructions manual for JSM IC848A. *JOEL Ltd*.


Appendix A: Thermal Conductivity Error Analysis

The rate of heat flow for a thermal model shown in figure A-1 can be written as,

The rate of heat flow in the structure can be written mathematically as,

\[ C_h \frac{\partial T_h}{\partial t} = -K_L(T_h - T_o) - K_B(T_h - T_s) + P_h \]  \hspace{1cm} (A-1)

\[ C_s \frac{\partial T_h}{\partial t} = -K_L(T_s - T_o) - K_B(T_s - T_h) + P_s \]  \hspace{1cm} (A-2)

where \( T_o, T_s \) and \( T_h \) are temperatures on frame, cold island and hot island respectively. \( C_h, C_s, P_h \) and \( P_s \) are the specific heats and power dissipated on hot and cold islands respectively. \( K_L \) and \( K_B \) are thermal conductance through the legs and through the bridge. For the steady state heat transport, the time dependent term vanishes and we get,

\[ 0 = -K_L(T_h - T_o) - K_B(T_h - T_s) + P_h \]  \hspace{1cm} (A-3)

\[ 0 = -K_L(T_s - T_o) - K_B(T_s - T_h) \]  \hspace{1cm} (A-4)
These equations are then solved as,

\[ T_h = T_o + \left( \frac{K_L + K_B}{(2K_B + K_L)K_L} \right)P \]  \hspace{1cm} (A-5)

\[ T_s = T_o + \left( \frac{K_B}{(2K_B + K_L)K_L} \right)P \]  \hspace{1cm} (A-6)

Equations A-5 and A-6 are simple first order linear equations with slopes of

\[ \frac{(K_L + K_B)}{(2K_B + K_L)K_L} \]  \hspace{1cm} (A-7)

and

\[ \frac{(K_B)}{(2K_B + K_L)K_L} \]  \hspace{1cm} (A-8)

respectively. Plots of \( T_h \) vs \( P \) and \( T_s \) vs \( P \) are straight lines. In general, a straight line is represented with an equation \( y = A + Bx \). The slope of a straight line is given as,

\[ B = \frac{N \sum xy - \sum x \sum y}{N \sum x^2 - (\sum x)^2} \]  \hspace{1cm} (A-9)
where $N$ is the number of data points, $x$ is the independent quantity and $y$ is the dependent variable. In our measurements, applied heating power ($P$) is the independent quantity plotted along $x$-axis and $T_h$ and $T_s$ are two dependent variables which are the temperatures measured on hot and cold islands plotted along $y$ axis (see figure A-1). We transform equation A-9 in terms of measured parameters and then it is written as,

$$m_h = \frac{N \sum PT_h - \sum P \sum T_h}{N \sum P^2 - (\sum P)^2}$$

(A-10)

and

$$m_s = \frac{N \sum PT_s - \sum P \sum T_s}{N \sum P^2 - (\sum P)^2}$$

(A-11)

where $m_h$ and $m_s$ are the slopes of $T_h$ vs $P$ and $T_s$ vs $P$ plots respectively. The error in the slope of a straight line is generally given as[107],

$$\delta B = \delta y \sqrt{\frac{N}{N \sum x^2 - (\sum x)^2}}$$

(A-12)

where $\delta B$ is the error in slope, $\delta y$ is the error in dependent variable, $N$ is the number of data points (or number of trials) and $x$ is the independent quantity along $x$ axis. According to this definition, in our measurements, the error in the slopes of $T_h$ vs $P$ and $T_s$ vs $P$ plots becomes,

$$\delta m_h = \delta T_h \sqrt{\frac{N}{N \sum P^2 - (\sum P)^2}}$$

(A-13)

and

$$\delta m_s = \delta T_s \sqrt{\frac{N}{N \sum P^2 - (\sum P)^2}}$$

(A-14)

where $\delta m_h$ and $\delta m_s$ are the errors in slope of $T_h$ vs $P$ and $T_s$ vs $P$ plots, $P$ is the applied power and $\delta T_s$ and $\delta T_s$ are the error in temperature measurements.

In our measurements, we measure temperature by measuring the the resistance of the
thermometer wires as a function of temperature. We then calibrate these thermometers by plotting temperature vs resistance and fitting a higher order polynomial to the curve. The slope of this curve in addition to the measurement resolution of the measuring instrument (SRS SIM 921) we find the error in temperature measurement.

In general it is written as,

\[ \delta T = \delta R \frac{dT}{dR} \]  

(A-15)

where \( \delta T \) is the error in temperature, \( dT/dR \) is the slope of \( T \) vs \( R \) plot and \( \delta R \) is the measurement resolution of the SRS SIM921. The measurement resolution usually vary with the measurement range and excitation voltage settings used during measurement. It is important to use the correct resolution according to the settings.

In this way we can define error in the two temperature measurements on two islands (\( \delta T_2 \) and \( \delta T_3 \)) and on frame (\( \delta T_1 \))as,

\[ \delta T_1 = \delta R \frac{dT_1}{dR_1} \]  

(A-16)

\[ \delta T_2 = \delta R \frac{dT_2}{dR_2} \]  

(A-17)

\[ \delta T_3 = \delta R \frac{dT_3}{dR_3} \]  

(A-18)

But the error in \( T_h \) and \( T_s \) is different because these are the change in temperature on the hot and cold island respectively with the temperature on frames and are written as,

\[ T_h = T_2 - T_1 \]  

(A-19)

\[ T_s = T_3 - T_1 \]  

(A-20)
Consequently, $\delta T_s$ and $\delta T_h$ becomes,

\[
\delta T_h = \sqrt{(\delta T_2)^2 + (\delta T_1)^2} \tag{A-21}
\]
\[
\delta T_s = \sqrt{(\delta T_3)^2 + (\delta T_1)^2} \tag{A-22}
\]

The thermal conductance through Si-N is calculated from the measured values of $P$, $T_h$, and $T_s$. If we simultaneously solve equations A-5 and A-6, we get equations for $K_B$ and $K_L$ as,

\[
K_B = \frac{P \Delta T_s}{(\Delta T_h - \Delta T_s)(\Delta T_h + \Delta T_s)} \tag{A-23}
\]
\[
K_L = \frac{P}{\Delta T_h + \Delta T_s} \tag{A-24}
\]

where $K_B$ and $K_L$ are thermal conductance through Si-N bridge and thermal conductance through legs in the thermal isolation platforms and $T_h$, and $T_s$ are the temperatures on hot and cold island respectively. The $\Delta$ is shows to show the change in these temperatures. We are mostly interested in thermal conductance through bridge. Equation A-23 can be written in terms of slopes $m_h$ and $m_s$. If we divide the numerator and denominator of equation A-23 by $P^2$, we get

\[
K_B = \frac{\Delta T_s}{P} \frac{1}{(\Delta T_h - \Delta T_s)(\Delta T_h + \Delta T_s)} \tag{A-25}
\]

which is equal to,

\[
K_B = \frac{m_s}{(m_h - m_s)(m_h + m_s)} \tag{A-26}
\]

Thus the fractional error in $K_B$ becomes,

\[
\frac{\delta K_B}{K_B} = \sqrt{\left(\frac{\delta m_s}{m_s}\right)^2 + \left(\frac{\delta (m_h - m_s)}{m_h - m_s}\right)^2 + \left(\frac{\delta (m_h + m_s)}{m_h + m_s}\right)^2} \tag{A-27}
\]
where $\delta K_B$ is the error in thermal conductance through bridge, $m_h$ and $m_s$ are the slopes of $T_h$ vs $P$ and $T_s$ vs $P$ plots respectively, and $\delta (m_h-m_s)$ & $\delta (m_h+m_s)$ are defined as,

$$
\delta(m_h - m_s) = \sqrt{(\delta m_h)^2 + (\delta m_s)^2} \quad (A-28)
$$

$$
\delta(m_h + m_s) = \sqrt{(\delta m_h)^2 + (\delta m_s)^2} \quad (A-29)
$$

which are essentially the same because they are absolute errors of difference and sum of slopes. Using equation A-27 error in thermal conductance can be written as,

$$
\delta K_B = \left(\sqrt{\left(\frac{\delta m_s}{m_s}\right)^2 + \left(\frac{\delta (m_h - m_s)}{m_h - m_s}\right)^2 + \left(\frac{\delta (m_h + m_s)}{m_h + m_s}\right)^2}\right)K_B \quad (A-30)
$$

Once the error is thermal conductance measurement is determined, we can calculate the error in thermal conductivity.

$$
\delta k = \left(\sqrt{\left(\frac{\delta K_B}{K_B}\right)^2 + \left(\frac{\delta l}{l}\right)^2 + \left(\frac{\delta w}{w}\right)^2 + \left(\frac{\delta t}{t}\right)^2}\right)k \quad (A-31)
$$

where $\delta k$ is the error in measured thermal conductivity, $\delta l, \delta w, \delta t$ are the errors in length and width of the bridge respectively. $\delta t$ is the error in the thickness. The well defined geometry of the bridge in thermal isolation platform eliminates errors from length and width and only the error in thermal conductance and thickness matters.

In case of a thermal conductance of a deposited film, we first calculate the individual error in thermal conductance before and after the film deposition and then the error in the substanation is calculated as,

$$
\delta K_s = \sqrt{(\delta K_B)^2 + (\delta K_{B'}^2)} \quad (A-32)
$$

where $\delta K_B$ is the thermal conductance of the background, $\delta K_{B'}$ is the thermal
conductance after the film deposition and \( \delta K_s \) is the thermal conductance of the sample. Now the error in thermal conductivity of the film can be determined using equation A-31 by replacing \( K_B \) and \( \delta K_B \) with \( K_S \) and \( \delta K_S \).
Appendix B: Thermopower:

Error Analysis

When we do thermopower measurements, we measure temperature on each island and the voltage across the film. The error in temperature measurement is calculated in a similar way as described in appendix A. Thermopower is determined by the slope of $\Delta V$ vs $\Delta T$ plot. A linear fit to the plot gives thermopower which is equal to,

$$\alpha = \frac{\Delta V}{\Delta T} \quad (B-1)$$

The error in slope is the error in the thermopower and given as,

$$\delta \alpha = \delta V \sqrt{\frac{N}{N \sum \Delta T^2 - (\sum \Delta T)^2}} \quad (B-2)$$

The error in the voltage measurement is determined by the resolution of the instrument used for the measurement range at which measurement is done. The voltage measurement resolution is $\delta V$. $N$ is the number of measurements and $\Delta T$ is the temperature difference between hot and cold islands. It is given as,

$$\Delta T = T_h - T_s \quad (B-3)$$
Then error in $\Delta T$ becomes,

$$\delta \Delta T = \sqrt{(\delta T_h)^2 + (\delta T_s)^2}$$  \hspace{1cm} (B-4)

where $\delta T_h$ and $\delta T_s$ are given by equations A-21 & A-22.
Appendix C: Miscellaneous

C-1 Alignment of bridge for film deposition

1. When you glue down the chip on the sample mount with silver paint, make sure it is well centered in the pocket (always use center pocket). If your chip is not a perfect square, then make your best guess.

2. Very carefully put the shadow mask on the pocket and hold it in place by atleast two screws. The screws in diagonal holes work best while aligning. Don not tighten the screws.

3. When you start aligning, move the microscope sample stage all the way to the back. This gives you enough room to move your sample around and towards you when you need to tighten the screws.

4. Align the bottom left alignment mark first, keep your finger on the mask, don’t push too hard. Move the microscope top to the left and align the second alignment mark on the chip.

5. Once you have both marks aligned, hold it there. Keep your finger on the mask and with other hand move the microscope sample stage very slowly towards you.

6. When the chip is perfectly centered in the pocket the top two alignment marks
are aligned automatically if we align the two bottom ones.

7. Now you can tighten the screw very slightly. Sometimes when we are tightening the screws, mask moves and mess up the alignment.

8. When you have tighten both screws, you can remove your finger from the mask.

9. Take a look at the alignment again. If it looks good, you can put the other two screws in.

10. In case, when the chip is not perfectly centered in the pocket, it is important to look at the alignment of bridge once you have two alignment marks in place.

11. In some extreme cases, you may have to re align the chip in the pocket by silver painting it again.

12. When you are satisfied with you alignment, leave the sample mount alone for an hour.

13. Come back and tap the sample mount gently on the table top. Check your alignment again, this is to make sure that the shadow mask does not shift during transfer and handing and your alignment is solid.

C-2 Growing $\alpha$-Si alloys

1. You should have the desired rate calculated using the densities of the silicon and the other material you are going to evaporate.

2. start heating up both sources together so that you don’t waste your one evaporating material while waiting for the rate of other.
3. Always enable log in SQS software for recording rate and thickness at every instant. This will help you estimating the composition, if the rate fluctuates during the deposition.