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Design of Power Switched-Capacitor Converters and Their Performance Analysis in a Soft-Charging Operation

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We proposed a high voltage gain and a very low output impedance power switched-capacitor converter (PSC) with a lower number of components compared to other step-up switched-capacitor topologies. The high output efficiency and the higher power density are two fundamental aspects of the PSC converter.

We can eliminate the current transient by applying the soft-charging technique that results a higher power density and a higher efficiency in PSC. The soft-charging operation is more preferable to the soft-switching technique (resonant operation) since it does not require any auxiliary components. Furthermore, soft-charging helps to resize capacitors and reduce the switching frequency of the PSC converter.

Furthermore, a split-phase control design is proposed to achieve the complete soft-charging operation in a PSC. The control diagram was designed for a 1-to-4 PSC (two levels of the PSC) which controls eight switches to exhibit eight modes of operation. The complete soft-charging accomplishes a 96% efficiency due to the lower output impedance and the dead time switching. LT-spice software has been used to verify the proposed control, and the results were compared with hard-charging and incomplete soft-charging operations.

In this research, we also proposed a two-level power switched-capacitor boost converter (PSC-boost) for a high voltage gain application by integrating a PSC converter and a conventional boost converter. The PSC switched-capacitors and the conventional boost converter are respectively cascaded as a primary and a secondary side of the proposed converter. Without alerting of the secondary side (conventional boost), the conversion ratio can be increased by adding more switched-capacitors cells. The proposed converter similarly acts as an MBC; however, it can maintain the rated voltage gain at a higher duty cycle. Unlike the MBC converter, the simulated voltage gain is closer to the calculated voltage gain for PSC-boost converter. In addition to the switched-capacitors insertion, a switched inductor model is used instead of the single inductor in the traditional boost converter. Five switches, five capacitors, seven diodes, and three inductors are used to build a PSC-boost switched-inductor converter. The PSC-boost converter accomplishes 94% efficiency which a higher rated power.

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Ayoob Alateeq

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Table of Contents

Abstract ii

Acknowledgements iv

List of Figures vii

List of Tables ix

CHAPTER ONE: INTRODUCTION 1
1.1 DC-to-DC converters 7
1.3 Slow-switching limit impedance of a 4-to-3 series to parallel SC converter 12
1.4 Problem Statement 15
1.5 Methodology 15
1.6 The Structure of the Dissertation 16

CHAPTER TWO: A SERIES OF POWER SWITCHED-CAPACITOR (PSC) CONVERTERS 17
2.1 Introduction 17
2.2 Power switched-capacitor (PSC) converter; topology and operation 18
2.3 Slow-switching limit impedance (**Rssl**) of the second order PSC converter 24
2.4 Fast-switching limit impedance of the second order PSC converter 30
2.5 Generalized power switched-capacitor converter 31
2.6 A comparison between the proposed PSC converter with three SC converter topologies 33

CHAPTER THREE: AN INCOMPLETE SOFT-CHARGING OPERATION OF THE SECOND ORDER PSC CONVERTER 36
3.1 Introduction 36
3.2 An incomplete soft-charging operation of the second order PSC 37
3.3 Slow-switching limit impedance (**Rssl**) of second order PSC converter at a complete soft-charging operation 42

CHAPTER FOUR: A COMPLETE SOFT-CHARGING OPERATION OF THE SECOND ORDER PSC CONVERTER 43
4.1 Introduction 43
4.2 A complete soft-charging operation of the second order PSC converter 43
4.3. Generalized split-phase control diagram of the power switched-capacitors converter 48
4.4. Slow-switching limit impedance (***Rssl***) for split-phase operation 49
4.5. Simulated results of the second order PSC converter at three different operation techniques 51
4.6 Numerical example 57
4.7 A simulated result of two-level PSC by using EMTP-RV software and LTspice 58

CHAPTER FIVE: PSC CONVERTER APPLICATION FOR HIGH GAIN PROVISION 62
5.1 Introduction 62
5.2 The proposed design MBC with switched inductor model 65
5.3 Modes of operation of MBC 65
5.3.1 Mode 1 65
5.3.2 Mode 2 65
5.4 Analysis of the proposed switched inductors boost converter 66
5.5 A comparison between the proposed MBC and two other MBC topologies 70
5.6 Using a PSC converter as a voltage multiplier for a DC-to-DC switched-inductor boost converter 74
5.7 Analysis of the proposed switched inductors model by using PSC cells as voltage multipliers 76
5.8 Modes of operation of PSC-boost converter 77
5.9 Analysis of the PSC-boost converter 79
5.10 Simulated results and a comparison of PSC-boost and MBC converter 82

CHAPTER SIX: CONCLUSION AND FUTURE WORK 86
6.1 Conclusion 86
6.2 Future Work 88

References 90

Appendix 105
List of Publications 105

List of Figures

Figure 1.1: Three step-up SC converter topologies (a) 1-to-4 Dickson (b) 1-to-4 ladder (c) 1-to-4 series-parallel 3
Figure 1.2: Output impedance of a typical SC converter.....4
Figure 1.3: A comparison of four SC converter topologies including the proposed PSC in the number of switches and capacitors 4
Figure 1.4: A conventional boost converter design. 8
Figure 1.5: A 4-to3 series to parallel SC converter [10].....9
Figure 1.6: A simulated LTspice result of a 4-to-3 series to parallel SC converter.....14

Figure 2.1: A 1-to-4 PSC topology (two-stage).....18
Figure 2.2: LTspice design of a 1-to-4 PSC topology (two-stage). 20
Figure 2.3: (a) Timing diagram of a 1-to-4 PSC topology; (b) four-mode operation of a 1-to-4 PSC converter. 22
Figure 2.4: The input and output voltages of a 1-to-4 and 1-to-2 of the proposed PSC converter. 23
Figure 2.5: Efficiency vs rated power of a 1-to-4 at 10V and 5V input. 23
Figure 2.6: A 1-to-8 PSC topology (three-stage). 24
Figure 2.7: The charge flow for the operation modes in the 1-to-4 PSC converter. 25
Figure 2.8: Switching frequency against the output voltage. 29
Figure 2.9: The 1-to-4 PSC efficiency at different capacitors' sizes. 30
Figure 2.10: a) voltage doubler converter b) a generalized control diagram of the PSC converter. 32
Figure 2.11: Two cascaded voltage doubler converters and formalized two stages of PSC converter. 33
Figure 2.12: The efficiency of four compared topologies at different rated power. 34
Figure 2.13: The output impedance of four compared topologies at different switching frequency.....34
Figure 2.14: A comparison between PSC and series to parallel topologies in maximum stress on switches 35
Figure 2.15: A comparison between PSC and series to parallel topologies in number of switches.....35

Figure 4.1: (a) A proposed timing diagram to achieve a complete soft-charging in the 1-to-4 PSC converter; (b) eight operation modes of the 1-to-4 PSC converter in the complete soft-charging technique. 45
Figure 4.2: The charge flow for the split operation modes in the 1-to-4 PSC converter…46
Figure 4.3: The 1-to-4 PSC topology with an output LC filter. 51
Figure 4.4: Simulation output impedance of the 1-to-4 PSC converter vs the switching frequency at three charging methods: hard-charging, incomplete soft-charging, complete soft-charging II. 53
Figure 4.5: Capacitor voltage mismatch during hard-charging between $VCf2 - VC2$ and $VCf2 - Vin$. 54

Figure 4.6: The elimination of the capacitor voltage mismatch during complete soft-charging II between VCf2 − VC2 and VCf2 − Vin. 54
L of LC filter.....55
Figure 4.7: The current waveform of Cf2 showing the transient in the hard-charging was eliminated by applying the complete soft-charging II. 56
Figure 4.8: The PSC converter efficiency vs the rated power at different operation techniques: hard-charging, incomplete soft-charging, complete soft-charging I, and complete soft-charging II (with LC filter). 56
Figure 4.9: The input and output voltages of a 1-to-4 and 1-to-2 of the proposed PSC converter by using LTspice and EMTP-EV simulators. 59
Figure 4.10: The efficiency of a 1-to-4 and 1-to-2 of the proposed PSC converter by using LTspice and EMTP-EV simulators. 60
Figure 4.11: The current transient at Cf2 hard-charging operation by using LTspice and EMTP-EV simulators. 60
Figure 4.12: The current transient at Cf2 is eliminated at complete soft-charging operation by using LTspice and EMTP-EV simulators. 61

Figure 5.1: The MBC with the proposed switched inductor.....63
Figure 5.2: Steady state waveforms in CCM with L1equal L2 and L3. 64
Figure 5.3: Mode 1 of the proposed three level MBC when S is on. 64
Figure 5.4: Mode 2 of the proposed three-level MBC when S is off. 67
Figure 5.5: Iinwith the duty cycle, shows L1, L2 and L3 parallel and series connections. 69
Figure 5.6: Duty cycle vs conversion ratio of the three MBC types.....71
Figure 5.7: Switch voltage stress versus voltage gain of proposed converter and compared, [85- 88] and [89-91] between 4 to 15 voltage gains. 72
Figure 5.8: Voutof the three compared MBC types.....72
Figure 5.9: Ioutof the three compared MBC types.....73
Figure 5.10: Poutof the three compared MBC types.....73
Figure 5.11: The 4-level MBC converter:.....76
Figure 5.12: The 2 levels of the proposed PSC-boost converter proposed in [100]. 77
Figure 5.13: a) The operation modes of the PSC-boost converter. b) Timing diagram of the PSC-boost converter. 79
Figure 5.14: The number of levels against the voltage gain at 50% duty cycle of the MBC converter and the PSC-boost. 84
Figure 5.15: The duty cycle against the voltage gain of the 4-level MBC converter and the 2-level PSC-boost. 84
Figure 5.17: The output impedance of the 2-level PSC boost and the 4-level-MBC at a different switching frequency. 85

List of Tables

Table 2.1: Simulation parameters of LTspice design 19
Table 2.2: Charge Flow for the 1-to-4 PSC converter 27
Table 2.3: Equation of the voltage stress on all semiconductors and capacitors. 31

Table 4.1: Simulation parameters of PSC to operate in hard- and soft-charging 55
Table 4.2: A comparison among three charging operations in output impedance calculations. 58
Table 4.3: Simulation parameters of LTspice and EMTP-RV simulators..... 59

Table 5.1: Conversion ratio of three different MBC types at ideal components assumption. 69
Table 5.2: Design Parameters Calculated by [70] 69
Table 5.3: A comparison between the proposed PSC-boost and the MBC converter. 81
Table 5.4: Simulation parameters of the PSC-boost and the MBC converter. 81
Table 5.5: Prices of each elements in Figure 5.11 and Figure 5.12 according to Digi-Key company……83

Abbreviations

DC "direct voltage"

EV "Electric Vehicle"

S-P "Series to Parallel"

SC "Switched-Capacitors"

SSL "Slow Switching Limit"

FSL "Fast Switching Limit"

$\mathbf{R_{ds\text{-}on}}$ "On Resistror of the MOSFET"

$\mathbf{R_{SS}}$ "Slow Switching Limit impedance"

$\mathbf{R_{FSL}}$ "Fast Switching Limit impedance"

PWM "Pulse-width modulated"

LNR "Line regulation"

η "Efficiency"

PSC "Power Switched-Capacitors"

$\boldsymbol{fsw}$ "Switching Frequency"

KCL "Kirchhoff's Current Low"

KVL "Kirchhoff's Voltage low"

MBC "Multilevel boost converter"

$\mathbf{V_{in}}$ "Input voltage"

$\mathbf{V_{out}}$ "Output voltage"

q "electric charge"

$\mathbf{q_{in}}$ "Input electric charge"

$\mathbf{q_{out}}$ "Output electric charge"

$\boldsymbol{a_c}$ “Charge multipliers of a capacitor”

$\boldsymbol{a_r}$ “Charge multipliers of the switch”

$\mathbf{A_i}$ “Reduced matrices loop”

$\mathbf{B_i}$ “Reduced incidence matrices”

CCM “Continuous conduction mode”

CHAPTER ONE: INTRODUCTION

DC-to-DC converters are commonly designed with magnetic elements for energy storing purposes. Designing a DC-to-DC converter with magnetic components such as an inductor leads to low power density due to the inductor bulky size. An increase in the power density of DC-to-DC converters requires a higher switching frequency (f_{sw}) since the inductor size is inversely proportionate to the switching frequency [1-3]. Increasing the f_{sw} can solve the problem partially; however, it will cause a switching loss produced by semiconductor elements. A growth in switching loss is conversely proportional to the converter efficiency [4][5]. High power density and high efficiency are two significant requirements for designing a DC-to-DC converter functional for tiny electronic circuit integration such as in battery electric vehicles (EV).

To satisfy these desires, the DC-to-DC switched-capacitors (SC) converters are widespread for EV. Because the DC-to-DC SC converters contain only capacitors and switches, they have a high-power density. The DC-to-DC SC converters come in many topologies such as, series to parallel [6-10], Dickson [11, 12], Fibonacci [13], ladder [14], and Voltage Doubler [15-20] where some of those are presented in Figure 1.1. Charging and discharging the capacitors allow the electric charge to flow from the input to the output to accomplish voltage regulation by alternating the switches' states. In addition to the high-power density, the SC converters tend to maintain the efficiency at a high voltage gain.

Because of their numerous topologies, analysis of the SC converters has been considered a challenging task. Several work tried to find a way to study and analyze the SC converters, such as [21-24]. Where in this work, the analysis in [5][25-26] has been applied. Two operation states occur in most types of SC converter, which are charging and discharging modes. The duty cycle of each mode is 50%. The DC-to-DC SC converter is simply a converter excluding inductor that operates to step up/down the voltage by changing the capacitor's terminals at high switching frequencies (f_{sw}). In the SC each capacitor terminal is connected to a number of switches, some of which operate in first mode while others work in the second mode. Changing the capacitor's connections to these two switches' operations allows electric charge q to flow in two different tracks, either to or from the capacitors. Raising power density using such a converter with only two types of components (switches and capacitors) is the main advantage of the SC converters. Moreover, SC converters have limited issues with electromagnetic interference because of the elimination of magnetic components such as the inductor. The number of capacitors and switches are selected regarding the conversion ratio and converter topology.

The total charge of the charging mode is assumed to equal the total charge in the discharging mode [5]. By studying and analyzing the charge flow, the SC converter voltage gain, the slow switching limit (SSL), and the fast switching limit (FSL) can be obtained. The output impedance at the SSL limit is proportional to the switching frequency and the capacitors' sizes while the output impedance at the FSL limit depends on the switches resistance R_{ds_on} [24]. Finding these two limits (SSL and FSL) helps to optimize the output impedance of the SC converter, and thus it would implement the efficiency. The desired value of the SSL limit is the intersection with the FSL limit asymptote as in Figure 1.2.

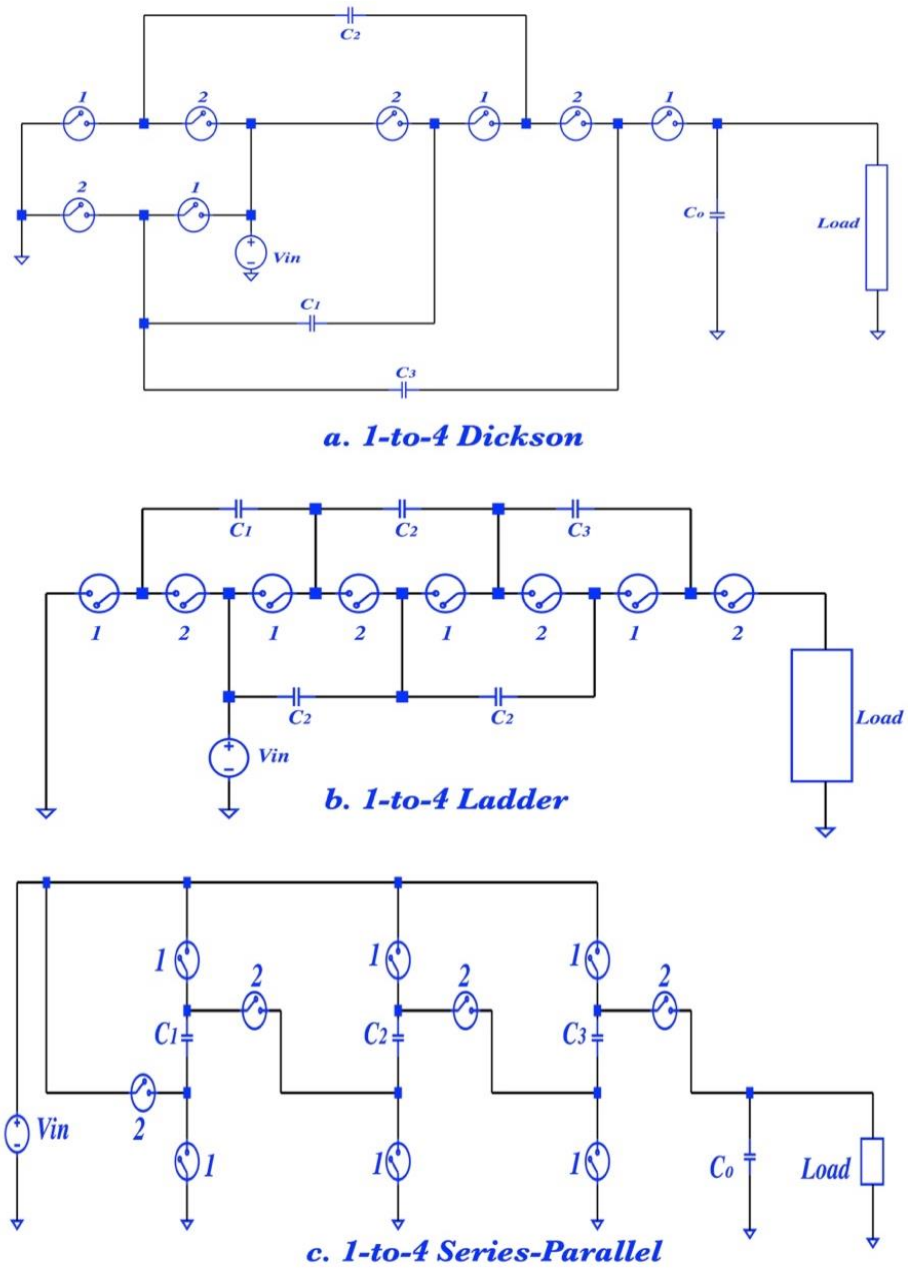


Figure 1.1: Three step-up SC converter topologies (a) 1-to-4 Dickson (b) 1-to-4 ladder (c) 1-to-4 series-parallel

However, the SC converters are not ideal or without drawbacks. For instance, providing a higher voltage gain is unlikely to be achieved with SC converters. Furthermore, the SC converters cannot normalize the output voltage in a lossless approach due to the

R_{ds_on} resistors. In this work, a switched-capacitors converter is proposed to step-up a DC-to-DC voltage [27][28]. The proposed SC converter is referred as a power switched capacitors (PSC) converter. As compared to other SC step up topologies the PSC provides a higher gain voltage at a smaller number of elements as in Figure 1.3

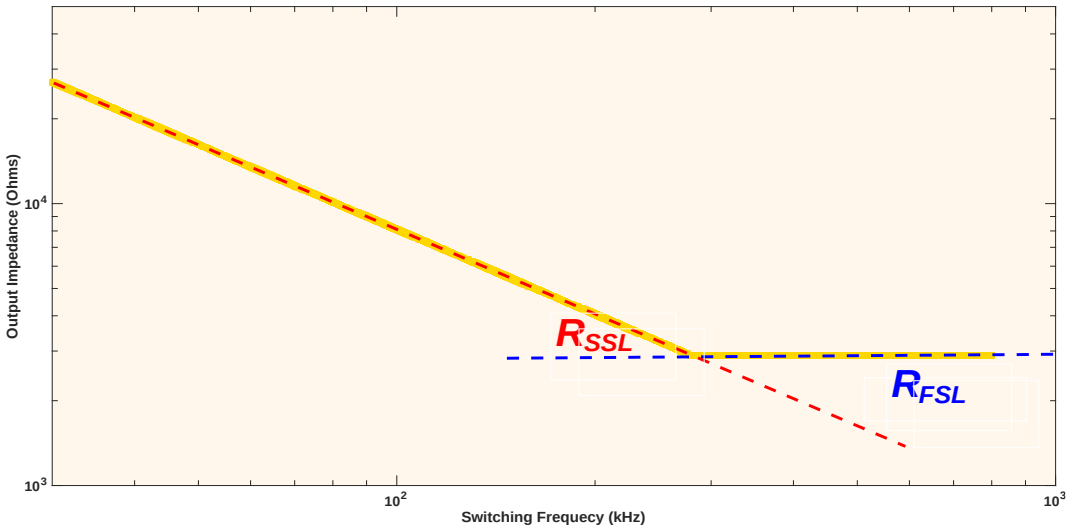


Figure 1.2: Output impedance of a typical SC converter

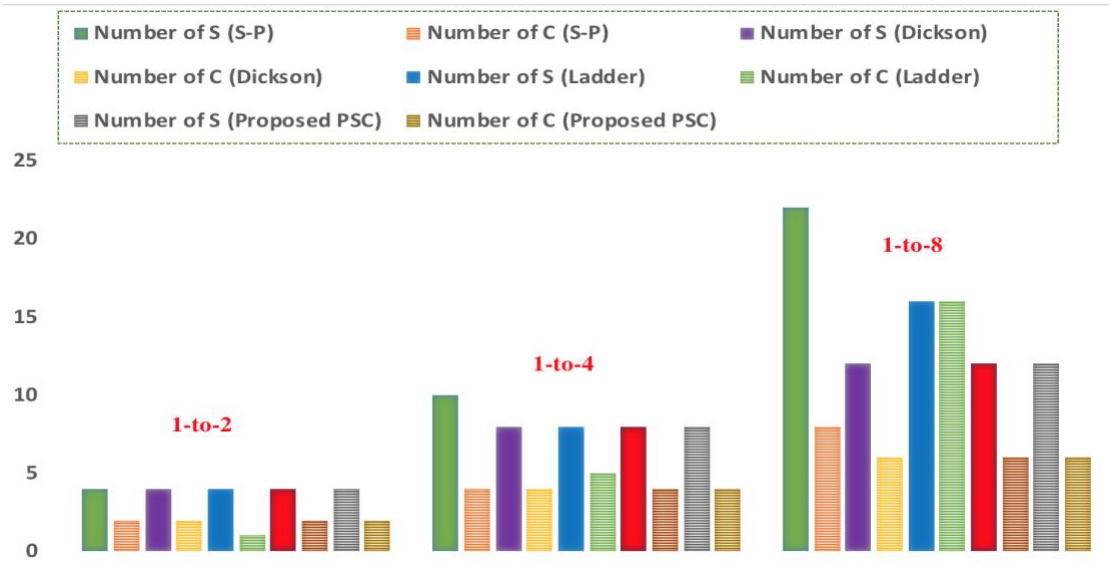


Figure 1.3: A comparison of four SC converter topologies including the proposed PSC in the number of switches and capacitors.

The PSC converter has a gain voltage of $V_{out} = 2^n V_{in}$ where n is the number of stages. Each added stage requires two additional capacitors and four more switches [28]. Unlike the other SC converters' topologies, the number of operation modes increase with the number of levels. Each level of the PSC converter has two operation modes. For instance, the 1-to-4 PSC converter (two-levels) as in Figure 1 operates in four operation modes, where three levels operate in six operation modes. To achieve a superior efficiency , it is recommended that SC converters are designed with resonant soft-switching techniques. However, designing resonant SC converters requires additional components and hence a reduction in the power density is possible In addition to that, soft-switching techniques require a higher switching frequency to achieve the magnetic elements reduction [29–41].

The work in [42–46] proposed an alternative way of soft switching which is called a soft-charging operation. The soft-charging can be defined as a study of the voltage change across any capacitor's terminals in the circuit to reduce its size requirement and locate the potential charge flow. In [42-46], the soft-charging technique was applied to a 4-to-1 Dickson SC converter. The main advantage of applying the soft-charging technique instead of soft-switching is it is not essential to add more components to optimize the overall efficiency; however, optimizing the efficiency can be done by resizing the capacitors and reducing the output impedance [45]. In addition to that, the soft-charging operation helps to eliminate the current transient and voltage mismatch between any two parallel capacitors. In conventional operation (hard-charging), there are two ways to reduce the current transient, either by large capacitors selection or a higher f_{sw}. However, these two implementations reduce the power density and the fundamental efficiency

respectively. To overcome the current transient issue, the complete soft-charging techniques are proposed to achieve that with a lower f_{sw} and smaller capacitors [42]. Resizing the capacitors in soft-charging techniques can be done theoretically by analyzing the voltage change and charge flow for each capacitor. In addition to resizing the capacitors, the output capacitor is eliminated in the soft-charging technique. Incomplete soft-charging and complete soft-charging are the two types of soft-charging. One significant difference between them is the complete soft-charging operation operates in a split-phase control diagram. The proposed control for Dickson SC converter in [42] splits each operation mode into two modes, which are the conventional modes besides the transition modes.

In this work, the complete soft-charging operation has been applied to the proposed PSC converter in [27]. A control diagram has been proposed to achieve a complete soft-charging in a 1-to-4 PSC converter. Achieving the complete soft-charging shows an output impedance reduction and a superior efficiency achievement to the 1-to-4 PSC converter. In addition, the split-phase successfully recovered the current transient. The reason for that is due to the dead time of the control diagram. However, reducing the capacitor size caused a high-output voltage ripple. To overcome the ripple issues, an output LC filter has been inserted into the 1-to-4 PSC converter.

The multilevel boost converter (MBC) is a boost converter contains voltage multiplier cells added to its output side in order to increase the output voltage. The conversion ratio could be increased by increasing its number of level where each additional level has two diodes and two capacitors. On the other hand, MBC has a drawback related to limited output power due to its lower output current. To overcome that, we proposed a

switched inductor model for the MBC to increase the output current and expand MBC's applications. Furthermore, the new PSC converter has been used as voltage multipliers and inserted to a conventional boost converter. The new PSC-boost converter works similar to the MBC boost converter where PSC cells were used instead of multilevel cells to increase the voltage gain.

1.1 DC-to-DC converters

The regulated voltage by a DC-to-DC converter is essential to run electronic elements that are used on daily appliances such as personal computers or automobile devices. Either a DC or AC input voltage has to be regulated to a DC voltage. Regarding the input type, an appropriate device such as a transformer, rectifier, or filters is used to regulate the input voltage to a DC voltage. A DC-to-DC converter is mainly based on three switching regulator categories which are the pulse-width modulated (PWM) DC-to-DC, the resonant converters, and the switched-capacitor DC-to-DC converters [47].

Several measurements are used to validate the DC-to-DC converter where the main important aspect is the converter power conversion efficiency which is based on the ratio of the output power to the input power. The general equation to calculate the efficiency can be derived as the following

$$\eta = \frac{P_{out}}{P_{in}} \times 100 \qquad (1.1)$$

In addition to the efficiency measurement, a measurement of the converter's strength to provide a supposed output voltage is another important parameter which is called the line regulation (LNR)

$$LNR = \frac{\Delta V_{out}}{\Delta V_{in}} \times 100 \qquad (1.2)$$

Similarly, a measurement of load strength to maintain the load current variation is another essential measurement in the DC-to-DC converter. Two popular types of the DC-to-DC converter are the buck DC-to-DC converter and the boost DC-to-DC converter. Two switching elements, transistor and diode are used to either step down or step up the input voltage in the buck and boost DC-to-DC converters respectively. The inductor will be charged when the transistor is on and where it will discharge when transistor is off. The diode state usually conflicts the transistor's state to allow the charge's delivery to the output. 4-to-3 series to parallel SC converter

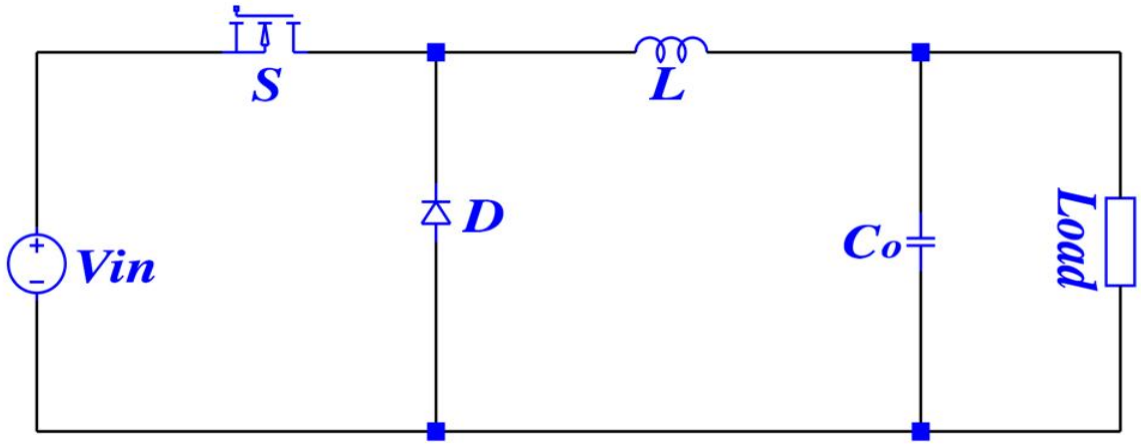


Figure 1.4: A conventional boost converter design.

A DC-to-DC switched-capacitor is an alternative converter to a traditional DC-to-DC converter with only switches and capacitors. The main advantage of the switched-capacitors converter is the absence of the magnetic elements such as inductors. In this section a 4-to-3 series to parallel SC converter will be discussed. Three capacitors and ten switches are used to build the proposed model. The duty cycle is 50% for each mode, 1 and

2, as shown in Figure 1.5. Charging modes S_1, S_4, S_5, S_7, S_8, and S_{10} are conducting; however, S_2, S_3, S_6, and S_9 are not. Charging modes C1, C2, and C3 are connected in parallel while they are in series in discharging mode. The total charge in charging mode equals the total charge of discharging mode [5] as in (1.3).

$$Q_T^1 = Q_T^2 \tag{1.3}$$

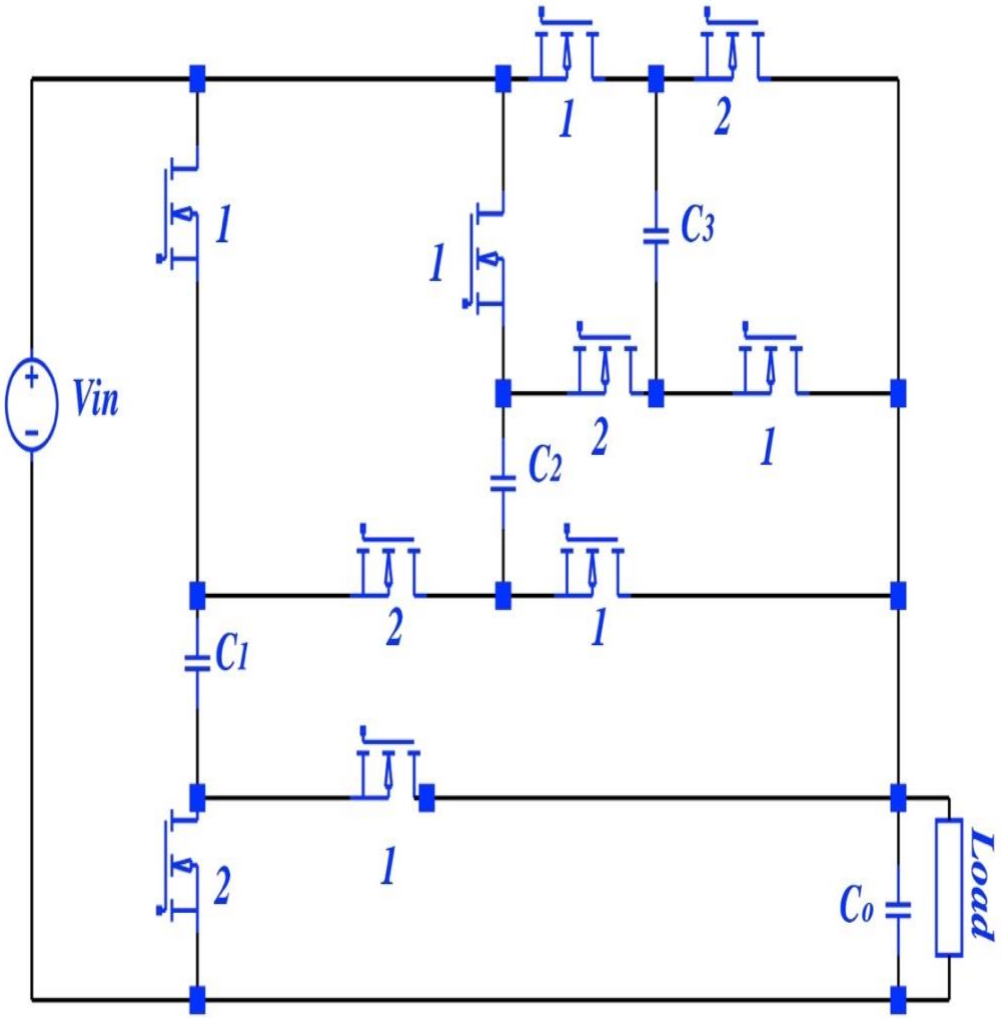


Figure 1.5: A 4-to3 series to parallel SC converter [10].

In mode-1 Figure 1-b, the voltage across C_1, C_2, and C_3 is the same because of the parallel connection (1.4).

$$V_1 = V_2 = V_3 = V_{in} - V_{out} \tag{1.4}$$

To satisfy (1.3) it is necessary to apply (1.4).

$$Q_T^1 = C_1V_1 + C_2V_2 + C_3V_3 + C_LV_{out} \tag{1.5}$$

by substituting (1.4) into (1.5) to get (1.6)

$$Q_T^1 = V_{in}(C_1 + C_2 + C_3) + V_{out}(C_1 + C_2 + C_3) + C_LV_{out} \tag{1.6}$$

In discharging mode, the V_{out} is the voltage total across each capacitor (1.7).

$$V_{out} = V_1 + V_2 + V_3 \tag{1.7}$$

The total charge of this mode is presented in (1.8).

$$Q_T^2 = C_1V_1 + C_2V_2 + C_3V_3 + C_LV_{out} \tag{1.8}$$

$$Q_T^2 = V_1(C_1 - C_2) + V_3(C_3 - C_2) + C_2V_{out} + C_LV_{out} \tag{1.9}$$

(1.9) has three unknown variables, so one more equation is needed to get (1.9) in V_{out} and V_{in} only. In mode-2, the streaming current in C_1, C_2, and C_3 are the same and can be calculated by (1.10)

$$ic_1 = C_1 \frac{dv1}{dt} = ic_2 = C_2 \frac{dv2}{dt} = ic_3 = C_3 \frac{dv3}{dt} \quad (1.10)$$

In this work, it is assumed that C_1, C_2, and C_3 have the same value (1.11).

$$dv1 = dv2 = dv3 \quad (1.11)$$

The rate of change in C_1, C_2, and C_3 is simply the voltage across the capacitor in mode-1 subtracted by the voltage across the capacitor in mode-2 (1.12) (1.13) (1.14).

$$dv1 = V_1^1 - V_1^2 \quad (1.12)$$

$$dv2 = V_2^1 - V_2^2 \quad (1.13)$$

$$dv3 = V_3^1 - V_3^2 \quad (1.14)$$

Where V_1^1 , V_2^1, V_3^1 are the voltages across C_1, C_2, and C_3 respectively during the charging mode, V_1^2 V_2^2 V_3^2 are their voltages in discharging mode. By rewriting (1.12) (1.13) (1.14), we get (1.15) (1.16) (1.17)

$$dv1 = V_{in} - V_{out} - V_1 \quad (1.15)$$

$$dv2 = V_{in} - V_{out} - V_2 \quad (1.16)$$

$$dv3 = V_{in} - V_{out} - V_3 \quad (1.17)$$

From (1.11), (1.15), (1.16) and (1.17) we can find a relationship between $V_1$and V_2 and between $V_1$and V_3 (1.18).

$$V_1 = V_2 = V_3 \tag{1.18}$$

By inserting (1.18) in (1.7) we get (1.19).

$$V_{out} = 3V_1 = 3V_2 = 3V_3 \tag{1.19}$$

Next, we substitute (1.19) into (1.9) to get Q_T^2 in one variable which is V_{out} (1.20).

$$Q_T^2 = \frac{V_{out}}{3}(C_1 - C_2) + \frac{V_{out}}{3}(C_3 - C_2) + C_2 V_{out} + C_L V_{out} \tag{1.20}$$

To get the conversion ratio of the proposed SC, we equate (1.6) with (1.20).

$$V_{in}(C_1 + C_2 + C_3) = \frac{4}{3} V_{out}(C_1 + C_2 + C_3)$$

$$\frac{V_{out}}{V_{in}} = \frac{3}{4} \tag{1.21}$$

(1.21) shows that the gain of the proposed design is 3/4 under a lossless component assumption.

1.3 Slow-switching limit impedance of a 4-to-3 series to parallel SC converter

Both capacitors and switches in the SC have losses related to either a switching, a charging, or a discharging of the switches and capacitors. This loss can be represented as an output impedance which is called a slow switching limit (SSL) impedance R_{ssl}. The conversion ratio in (1.21) is independent of capacitor size and also of f_{sw} of the design. Studying the charge flow for both modes as shown in Figure 1.5 and in order to calculate the charge multiplier for each capacitor a_c (1.22) [5]

$$q_c = a_c q_{out} \tag{1.22}$$

The input charge of mode-1 q_{in} is divided into three input charges, and each one flows through each of the parallel capacitors $q_{in}/3$. For mode-2 the input current is $-q_{in}/3$ so the charge flow in C_1, C_2, and C_3 in both mode-1 and mode-2 are represented in (21) and (22).

$$q_c^1 = \begin{bmatrix} q_{in}/3 \\ q_{in}/3 \\ q_{in}/3 \end{bmatrix} \tag{1.23}$$

$$q_c^2 = \begin{bmatrix} -q_{in}/3 \\ -q_{in}/3 \\ -q_{in}/3 \end{bmatrix} \tag{1.24}$$

The total output charge (1.25)

$$q_{out} = q_{out}^1 + q_{out}^2 = q_{in} + q_{in}/3 \tag{1.25}$$

by inserting (1.25) into (1.23) and (1.24) to get (1.26) and (1.27)

$$q_c^1 = \begin{bmatrix} q_{out}/4 \\ q_{out}/4 \\ q_{out}/4 \end{bmatrix} \tag{1.26}$$

$$q_c^2 = \begin{bmatrix} -q_{out}/4 \\ -q_{out}/4 \\ -q_{out}/4 \end{bmatrix} \tag{1.27}$$

by inserting (1.22) into (1.26) and (1.27) to get (1.28) and (1.29)

$$a_c^1 = \begin{bmatrix} 1/4 \\ 1/4 \\ 1/4 \end{bmatrix} \tag{1.28}$$

$$a_c^2 = \begin{bmatrix} -1/4 \\ -1/4 \\ -1/4 \end{bmatrix} \tag{1.29}$$

by using Tellegen's theorem [5][9], to find R_{ssl} of our proposed design (1.30).

$$\frac{V_{out}}{q_{out}} + \sum_{i=1}^{number\ of\ C} \frac{(a_{c,i})^2}{C_i} = 0 \tag{1.30}$$

where $\frac{V_{out}}{q_{out}} = R_{ssl}$

$$R_{ssl} = \frac{1}{16 f_{sw}} \left[\frac{1}{C1} + \frac{1}{C2} + \frac{1}{C3} \right] \tag{1.31}$$

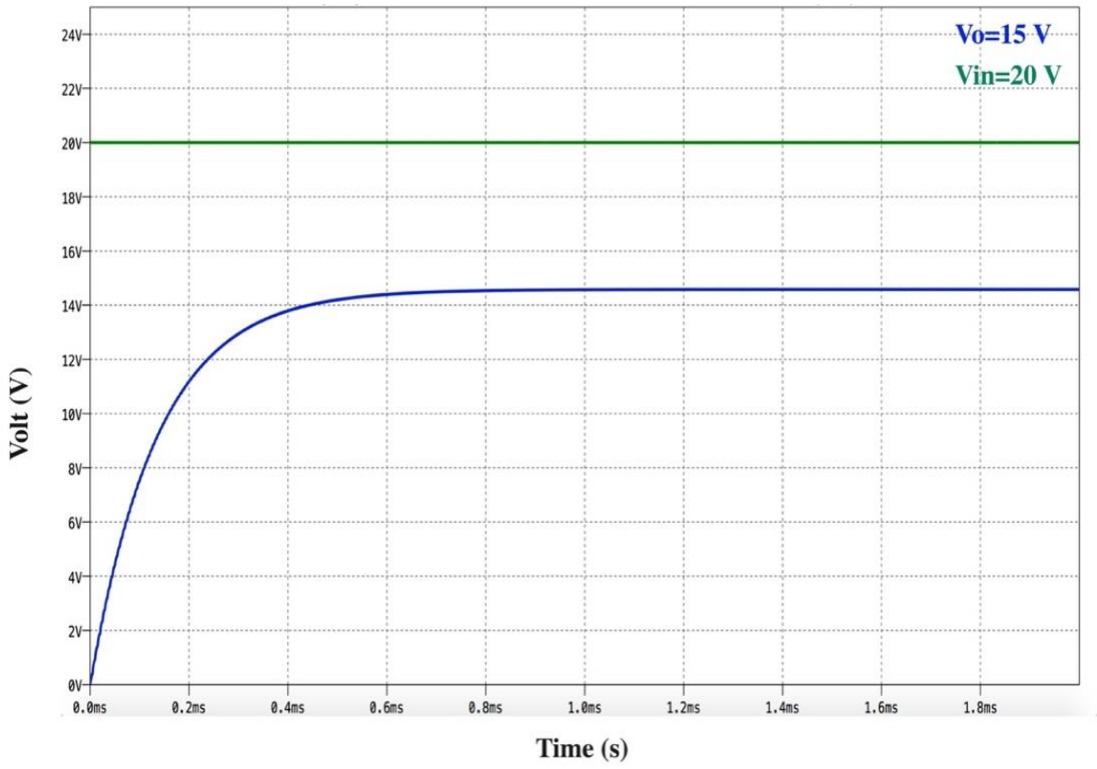


Figure 1.6: A simulated LTspice result of a 4-to-3 series to parallel SC converter.

1.4 Problem Statement

In addition to the discussion in section 1.1, how should a DC-to-DC converter's power density be increased and meet the small electronic circuit reequipment? DC-to-DC converters that contain magnetic elements require a higher switching frequency in order to minimize the magnetic sizes; however, this increase could affect their efficiency. The switched-capacitor converters are recommended instead due to the absence of magnetic elements. The most challenging task in designing SC converters is to maintain the efficiency and the number of elements at a higher voltage gain. The PSC converter has proven its efficiency and ability to provide a high voltage gain with a smaller number of elements. To improve the efficiency of the DC-to-DC converters, adding the resonant branches to achieve a soft switching operation is highly recommended. However, adding additional elements could affect the power density which is the fundamental aspect of SC converters. Instead of applying the soft switching operation, a soft-charging operation is more appropriate for SC converters due to the possibility of unnecessary insertion of additional components. Besides the efficiency improvement, the soft-charging operation helps to decrease the output impedance.

1.5 Methodology

The LTspice software simulation program is the main program used to analyze our model and study its performance in the soft-charging operation. The EMTP-RV program was used to validate the study of the soft-charging operation. The SIMULINK MATLAB was used to study the efficiency and analyze the voltage gain of the proposed model in

Chapter Five. The outcome results of this dissertation have been validated by publication of a MDPI journal paper and several conference papers (IEEE and SPIE).

1.6 The Structure of the Dissertation

The next chapters of the dissertation are ordered as follows:

- Chapter two talks about the proposed power switched-capacitor converter and how it operates when two stages are selected. It also includes the calculation and derivation of the voltage gain, output impedance, and capacitor selection by applying the charge flow and voltage change. At the end of this chapter is a comparison between the proposed PSC and other SC topologies, in the efficiency and output impedance.
- Chapter three includes an incomplete soft-charging operation of the second order PSC converter. The analysis was applied to the PSC converter in order to resize the capacitors and reduce the output impedance.
- Chapter four contains a study of a complete soft-charging operation in the second stage of the PSC. This chapter also includes a proposed control diagram to satisfy the split phase operation. Besides that, a generalization of the split phase operation is discussed. The implementations to the PSC efficiency and output impedance after applying the complete soft-charging operation are proven in this chapter.
- Chapter five shows an application of the PSC converter to be used as voltage multiplier cells in the non-isolated DC-to-DC converter. The proposed converter acts similar to the MBC converter with some privileges.
- Chapter six contains the dissertation's summary and details future work. Also, some of my publications are listed in this chapter.

CHAPTER TWO: A SERIES OF POWER SWITCHED-CAPACITOR (PSC) CONVERTERS

2.1 Introduction

Regarding the market's demand for a large voltage gain conversion, a single stage boost converter could not achieve a higher efficiency due to its duty cycles limits. To overcome a high gain requirement, designing two-stage converters has promised for being an efficient substitute for a traditional boost converter. The two-stage converter is based on using a SC converter as one stage where the other stage is a traditional boost converter. Several topologies of SC have been presented in previous chapter; however, most of those topologies require a large number of components to provide a higher voltage gain converter [48-50]. A proposed step-up power switched-capacitors (PSC) converter is presented in this chapter to fulfill the high voltage gain requirement [27]. The PSC converter successfully increases the voltage gain with a smaller number of elements and a lower voltage stress in switches. The procedure to analyze and obtain the voltage gain, output impedance limits, and capacitor sizes for the proposed PSC converter are discussed in this chapter under a steady state assumption. Efficiency calculations must be performed to determine the power of the SC converter.

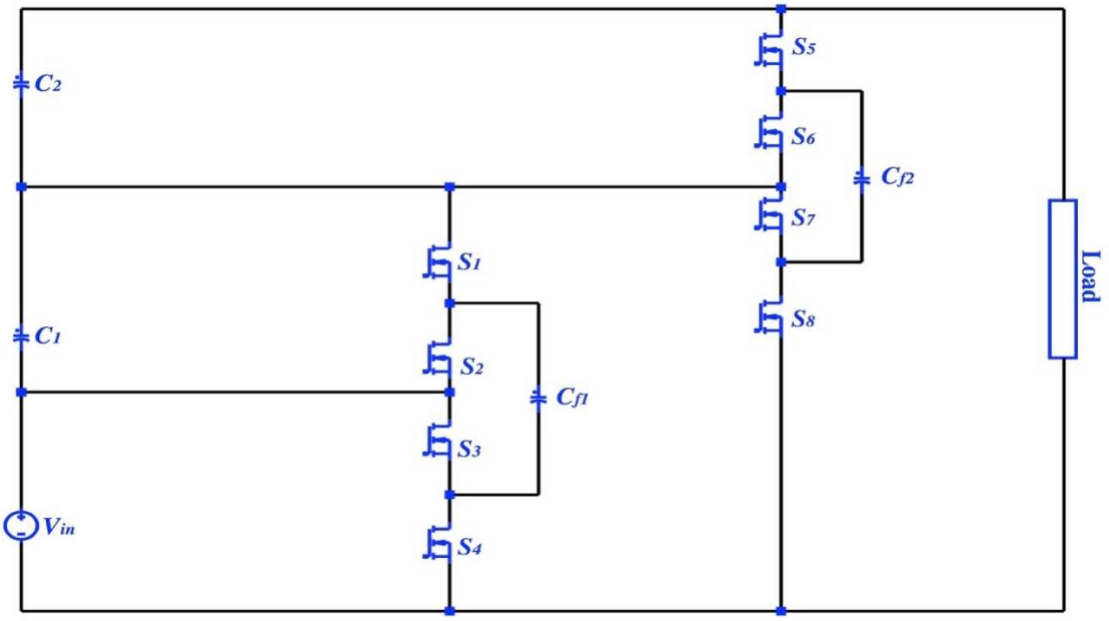


Figure 2.1: A 1-to-4 PSC topology (two-stage).

2.2 Power switched-capacitor (PSC) converter; topology and operation

This section introduces the topology of the proposed power switched-capacitor converter. Figure 2.1 shows a two-stage topology of the 1-to-4 PSC converter which produces an output voltage equals to $4V_{in}$.The first level contains four switches, S_1 S_2S_3 and S_4 , and two capacitors which are the bypass capacitor C_1 and flying capacitor C_{f1}. Similar to the first stage, the second level contains four switches, S_5 S_6S_7 and S_8 , and two capacitors; one of them is a bypass capacitor C_2 where the other capacitor is a flying capacitor C_{f2}. Two control groups are needed to control the two levels of the PSC converter as shown in Figure 2.3a. The first and second groups have a $\frac{T}{4}$ phase shift, wherein each

group a $\frac{T}{2}$ phase shift is between its two control signals. The input voltage is doubled at first stage where this doubled voltage will be doubled again at the second level.

The flying capacitors are either in parallel to the input source or to the bypass capacitors to pump the electric charge from the input to the output [51]. Related to the control diagram, four modes of operations are possible (Figure 2.3b). These operation modes come in the following sequence: Mode-1, Mode-2, Mode-3, Mode-4, and Mode-1. In each mode, the capacitors are connected differently for voltage regulation purposes. In Mode-1 the flying capacitor C_{f1} is charging; however, flying capacitor C_{f2} is discharging. In Mode-2, both flying capacitors C_{f1} and C_{f2} are discharging, whereas they are both charging in Mode-4. In Mode-3 C_{f1} is discharging whereas C_{f2} is charging.

A LTspice design of the two stage PSC converter was designed with simulation parameters as in Table 2.1. Figure 2.2 shows a LTspice design of a 1-to-4 PSC topology (two-stage).

Parameter	Value
$\boldsymbol{V_{in}}$	10 V
$\boldsymbol{f_{sw}}$	200 KHz
$\boldsymbol{C_{f1}C_{f2}}$	188 µF
$\boldsymbol{C_1C_2}$	94 µF
$\boldsymbol{R_L}$	20
Switches	IPB075N04L

Table 2.1: Simulation parameters of LTspice design

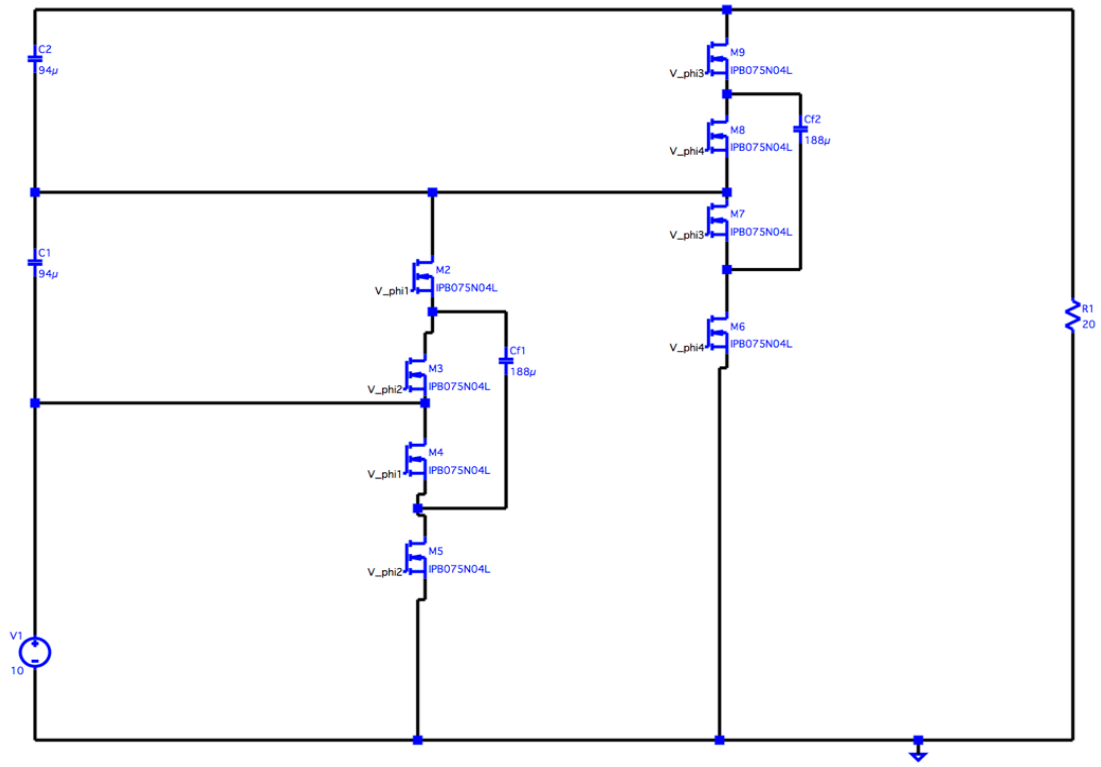


Figure 2.2: LTspice design of a 1-to-4 PSC topology (two-stage).

To find the voltage gain of the proposed converter, charge balance analysis is applied instead of discrete-time analysis as in [52][53]. Each mode has a total charge that can be derived from the following equations:

$$QT_i = V_{C_1}C_1 + V_{C_2}C_2 + V_{C_{f1}}C_{f1} + V_{f2}C_{f2} \tag{2.1}$$

where i is the number of modes 1, 2, 3 and 4 (from Mode-1 Figure 2.3).

$$V_{C_{f1}} = V_{C_1}$$

$$V_{C_2} = V_{C_{f2}} \tag{2.2}$$

$$V_{C_{f1}} = V_o - V_{in} - V_{C_{f2}} \quad (2.3)$$

by substituting (2.2), (2.3) and (2.4) in (2.1) we get the total charge of Mode-1 (2.5)

$$QT_1 = V_{in}(-C_{f1} - C_1) + V_{f2}(C_2 + C_{f2} - C_1 - C_{f1}) + V_o(C_1 + C_{f1}) \quad (2.4)$$

To find the total charge of the rest of the modes, the same steps can be repeated

$$QT_2 = V_{in}(C_{f1} - C_1) + V_{f2}(C_1 + C_{f2} - C_2) + V_{out}C_2 \quad (2.1)$$

$$QT_3 = V_{in}(-C_{f1} - C_1) + V_{f2}(C_1 + C_{f1} + C_{f2} - C_2) + V_{out}C_2 \quad (2.2)$$

$$QT_4 = V_{in}(C_{f1} - C_1) + V_{f2}(-C_1 + C_{f2} + C_2) + V_{out}C_1 \quad (2.3)$$

In the steady state operation, the total charge of any two modes is assumed to be equal. In this work, we assumed that

$$QT_1 = QT_4 \quad (2.4)$$

$$QT_2 = QT_3 \quad (2.5)$$

By simplifying (2.8) and (2.9) we get

$$2V_{in}C_{f1} + V_{f2}C_{f1} - V_{out}C_{f1} = 0 \quad (2.6)$$

$$2V_{in}C_{f1} - V_{f2}C_{f1} = 0 \quad (2.7)$$

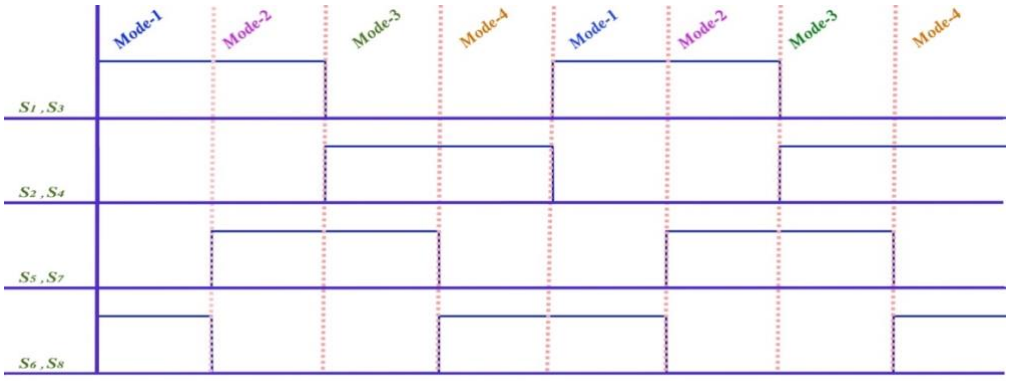
By combining (2.10) and (2.11), the 1-to-4 PSC converter's voltage gain can be calculated (2.12)

$$V_{out} = 4V_{in} \quad (2.8)$$

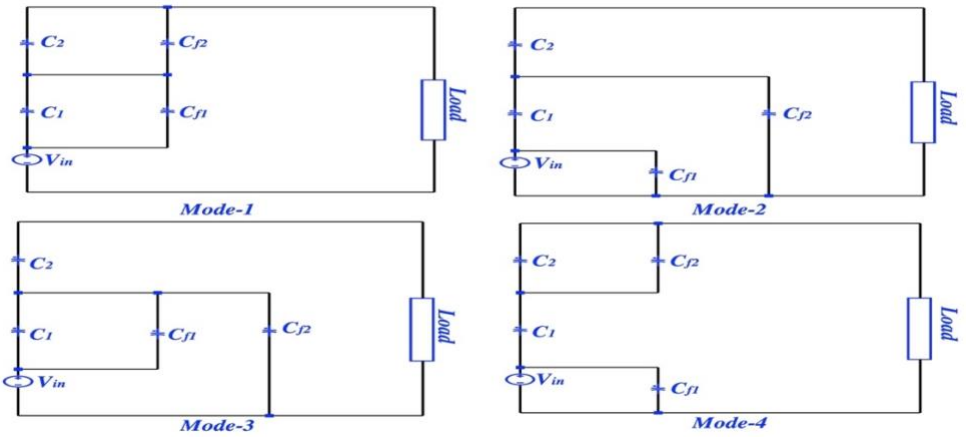
The general form of the proposed converter is

$$V_{out} = 2^n V_{in} \tag{2.9}$$

where n is the number of the stage. The output voltages of the stage one and stage two of the PSC converter are presented in Figure 2.4. The converter efficiency at two different input voltages is presented in Figure 2.5



(**a**)



(**b**)

Figure 2.3: (a) Timing diagram of a 1-to-4 PSC topology; (b) four-mode operation of a 1-to-4 PSC converter.

For each added stage, two capacitors and four switches are needed. Figure 2.6 presents three stages of the proposed converter with 1-to-8 conversion ratio, each switch operates in a 50% duty cycle whereas a $\frac{1}{2n}$ is phase shift between any two stages.

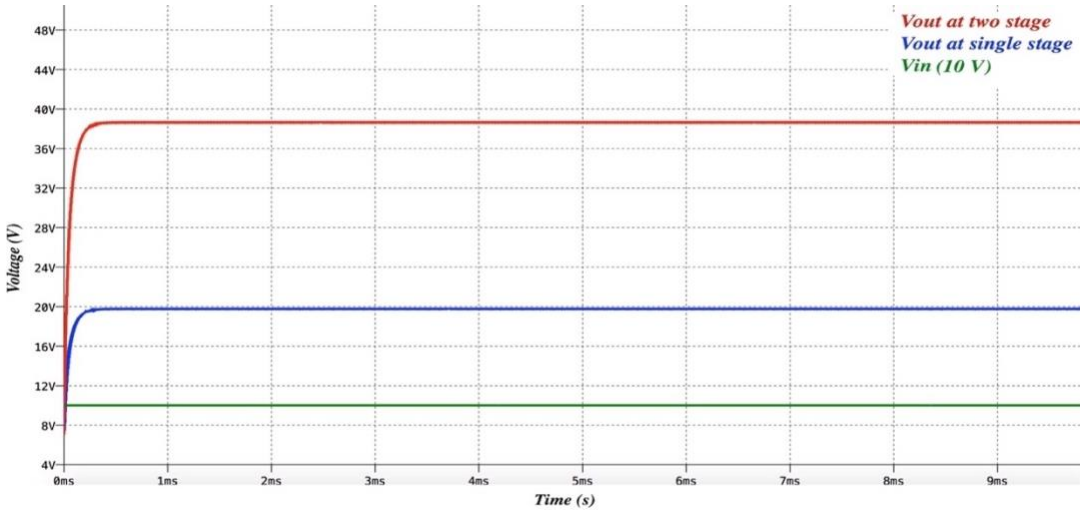


Figure 2.4: The input and output voltages of a 1-to-4 and 1-to-2 of the proposed PSC converter.

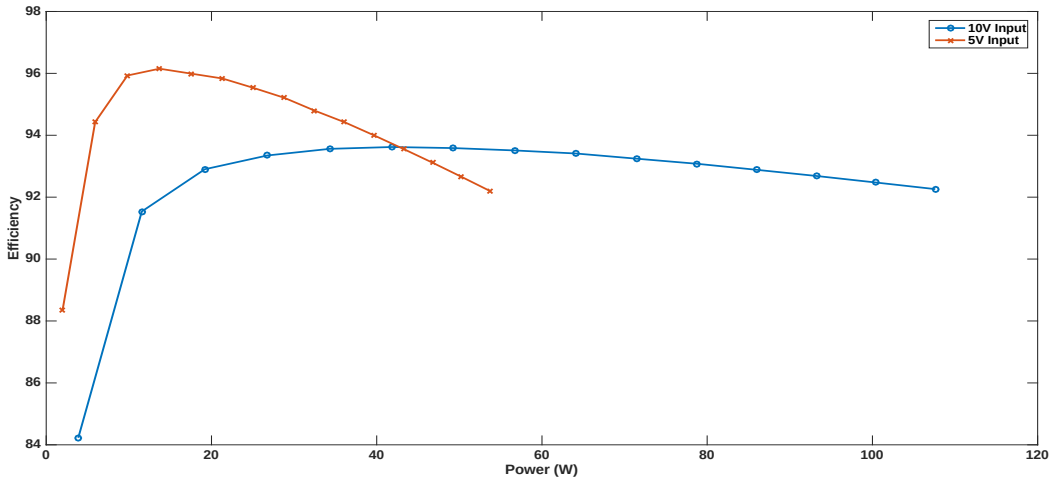


Figure 2.5: Efficiency vs rated power of a 1-to-4 at 10V and 5V input.

2.3 Slow-switching limit impedance (R_{ssl}) of the second order PSC converter

The SC converters suffer from losses related to the switches and the capacitors' charging or discharging process. This capacitors' loss can be characterized as an output impedance that is called a slow switching limit impedance, R_{ssl}. The charge flow analysis of the four modes has been applied to find the charge multiplier of the four capacitors a_c^i

$$q_c^i = a_c^i \, q_{out} \tag{2.10}$$

$$q_c = [q_{C_1} q_{C_2} q_{C_{f1}} q_{C_{f2}}]^T \tag{2.11}$$

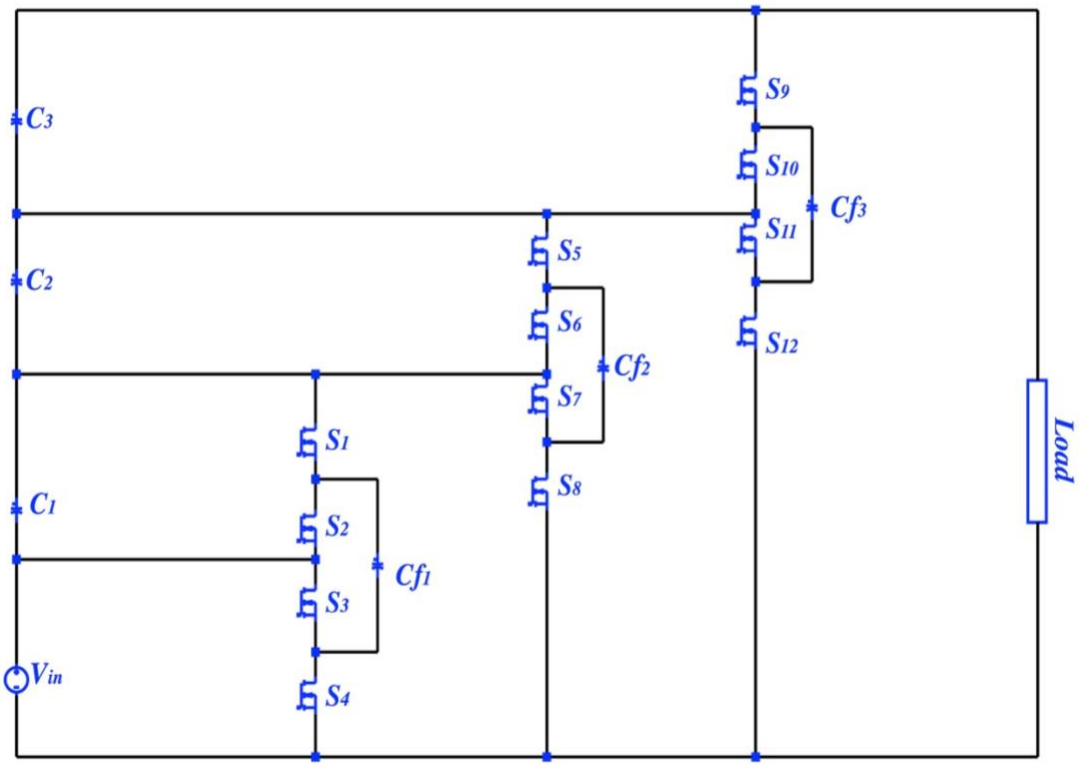


Figure 2.6: A 1-to-8 PSC topology (three-stage).

In [42-46] a useful technique was used to find the charge flow vectors of all the operation modes. For the *i*th mode, Kirchhoff's Current Low (KCL) can be derived by (2.16)

$$B_i q^i = 0 \tag{2.12}$$

where B_i is reduced incidence matrices of the four modes of 1-to-4 PSC converter. Each row in B_i corresponds to an independent KCL equation. The number of independent KCL equations can be derived by the number of nodes. Each element in the circuit has two nodes related to its positive and negative terminals as in Figure 2.7 [54][55]. The charge follow's direction is inspected as in Table 2.2.

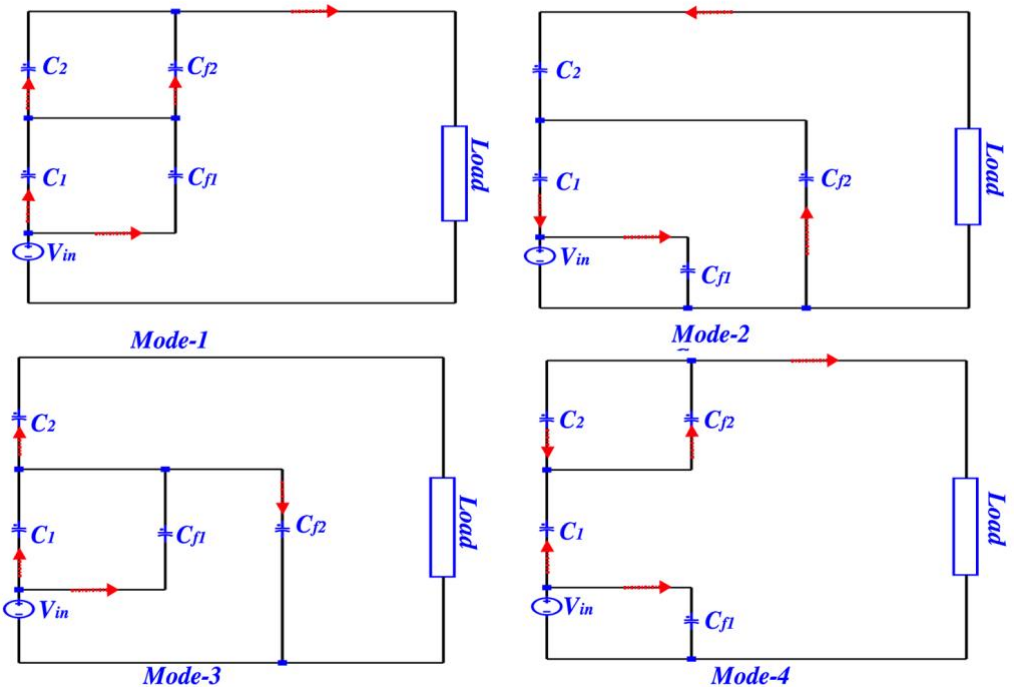


Figure 2.7: The charge flow for the operation modes in the 1-to-4 PSC converter.

$$B_{1,a} = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 0 & -1 & 1 \\ 1 & 0 & 0 & 0 & 0 & -1 \end{bmatrix}$$

$$B_{2,a} = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & -1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & -1 & -1 & 1 \end{bmatrix}$$

$$B_{3,a} = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & -1 & -1 \end{bmatrix}$$

$$B_{4,a} = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & -1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & -1 & 1 \\ 1 & 0 & 0 & -1 & 0 & -1 \end{bmatrix} \quad (2.13)$$

To find the charge flow's vectors, (2.17) can be solved for q^i.

$$q^1_{Flow} = \begin{bmatrix} 3 \\ 1 \\ 1 \\ 2 \\ 2 \\ 3 \end{bmatrix} q^2_{Flow} = \begin{bmatrix} -3 \\ -1 \\ -1 \\ -2 \\ -2 \\ -1 \end{bmatrix}$$

$$q^3_{Flow} = \begin{bmatrix} 3 \\ 1 \\ 1 \\ 2 \\ 2 \\ 1 \end{bmatrix} q^4_{Flow} = \begin{bmatrix} -3 \\ -1 \\ -1 \\ -2 \\ -2 \\ -1 \end{bmatrix} \quad (2.14)$$

Mode 1		Mode 2		Mode 3		Mode 4	
$\boldsymbol{q_{C1}^1}$	$\frac{q_{in}}{3}$	$\boldsymbol{q_{C1}^2}$	$\frac{-q_{in}}{3}$	$\boldsymbol{q_{C1}^3}$	$\frac{q_{in}}{3}$	$\boldsymbol{q_{C1}^4}$	$\frac{-q_{in}}{3}$
$\boldsymbol{q_{C2}^1}$	$\frac{q_{in}}{3}$	$\boldsymbol{q_{C2}^2}$	$\frac{-q_{in}}{3}$	$\boldsymbol{q_{C2}^3}$	$\frac{q_{in}}{3}$	$\boldsymbol{q_{C2}^4}$	$\frac{-q_{in}}{3}$
$\boldsymbol{q_{Cf1}^1}$	$\frac{2q_{in}}{3}$	$\boldsymbol{q_{Cf1}^2}$	$\frac{-2q_{in}}{3}$	$\boldsymbol{q_{Cf1}^3}$	$\frac{2q_{in}}{3}$	$\boldsymbol{q_{Cf1}^4}$	$\frac{-2q_{in}}{3}$
$\boldsymbol{q_{Cf2}^1}$	$\frac{2q_{in}}{3}$	$\boldsymbol{q_{Cf2}^2}$	$\frac{-2q_{in}}{3}$	$\boldsymbol{q_{Cf2}^3}$	$\frac{2q_{in}}{3}$	$\boldsymbol{q_{Cf2}^4}$	$\frac{-2q_{in}}{3}$
$\boldsymbol{q_{out}^1}$	q_{in}	$\boldsymbol{q_{out}^2}$	$\frac{-q_{in}}{3}$	$\boldsymbol{q_{out}^3}$	$\frac{q_{in}}{3}$	$\boldsymbol{q_{out}^4}$	$\frac{-q_{in}}{3}$

Table 2.2: Charge Flow for the 1-to-4 PSC converter

The total output charge with respect to the output charge can be found in (2.18)

$$q_{out,total} = q_{out}^1 + q_{out}^2 + q_{out}^3 + q_{out}^4 \tag{2.15}$$

The total output charge with respect to the input charge is

$$q_{out,total} = q_{in} + \frac{q_{in}}{3} + \frac{q_{in}}{3} + \frac{q_{in}}{3} = 2q_{in} \tag{2.16}$$

By using (2.21), (2.19) can be rewritten with respect to the output charge of the capacitors and the load (2.22)

$$q^1 = \begin{bmatrix} \frac{q_{out}}{2} \\ \frac{q_{out}}{2} \\ q_{out} \\ q_{out} \\ \frac{3q_{out}}{2} \end{bmatrix} q^2 = \begin{bmatrix} \frac{-q_{out}}{2} \\ \frac{-q_{out}}{2} \\ -q_{out} \\ -q_{out} \\ \frac{-q_{out}}{2} \end{bmatrix}$$

$$q^3 = \begin{bmatrix} \frac{q_{out}}{2} \\ \frac{q_{out}}{2} \\ q_{out} \\ q_{out} \\ \frac{q_{out}}{2} \end{bmatrix} q^4 = \begin{bmatrix} \frac{-q_{out}}{2} \\ \frac{-q_{out}}{2} \\ -q_{out} \\ -q_{out} \\ \frac{-q_{out}}{2} \end{bmatrix} \tag{2.17}$$

By dividing (2.21) by (2.15), the charge multipliers are presented in (2.23)

$$a^1 = \begin{bmatrix} \frac{1}{2} \\ \frac{1}{2} \\ 1 \\ 1 \\ \frac{3}{2} \end{bmatrix} a^2 = \begin{bmatrix} \frac{-1}{2} \\ \frac{-1}{2} \\ -1 \\ -1 \\ \frac{-1}{2} \end{bmatrix}$$

$$a^3 = \begin{bmatrix} \frac{1}{2} \\ \frac{1}{2} \\ 1 \\ 1 \\ \frac{1}{2} \end{bmatrix} a^4 = \begin{bmatrix} \frac{-1}{2} \\ \frac{-1}{2} \\ -1 \\ -1 \\ \frac{-1}{2} \end{bmatrix} \quad (2.18)$$

Then by applying the Tellegen's theorem to the PSC converter, in its four modes of operation, concludes $a^1.V^1$=$a^2.V^2 = a^3.V^3 = a^4.V^4 = 0$, R_{ssl} limit of the output impedance can be found for our proposed design (2.23).

$$V_{out}(a^1_{out} + a^2_{out} + a^3_{out} + a^4_{out}) + \sum_{capacitors} a^1_{ci}V^1_{ci} + a^2_{ci}V^2_{ci} + a^3_{ci}V^3_{ci} + a^4_{ci}V^4_{ci} = 0 \quad (2.23)$$

By recalling the output charge multipliers total $(a^1_{out} + a^2_{out} + a^3_{out} + a^4_{out})$ =3, and due to the periodic cycles, $\Delta V^i = (V^1_{ci} - V^2_{ci}) = (V^3_{ci} - V^4_{ci})$ and $a_{ci} = a^1_{ci}$= $-a^2_{ci}$ and $a_{ci} = a^3_{ci}$ =$-a^4_{ci}$ are assumed. By rewriting (2.23) into (2.24).

$$3V_{out}q_{out} + \sum_{capacitors} \Delta V^i q_i = 0 \quad (2.24)$$

Where the capacitors' voltage ripple is represented as $\Delta V^i = q_i/2C_i$, then by dividing by ${q_{out}}^2$ then

$$\frac{3V_{out}}{q_{out}} + \sum_{i=1}^{number\ of\ C} \frac{(a_{c,i})^2}{2C_i\ fsw} = 0 \tag{2.25}$$

where $\frac{V_{out}}{q_{out} fsw} = R_{ssl}$

$$R_{ssl} = \frac{1}{6}\sum_{i=1}^{number\ of\ C} \frac{(a_{c,i})^2}{C_i\ fsw} \tag{2.26}$$

R_{ssl} represents the charging and discharging loss caused by the capacitors. Based on (2.2 two possible ways to reduce R_{ssl} impedance either by increasing C_i or fsw. Figure 2.8 a Figure 2.9 show the increase in C_i and fsw optimized the output voltage and efficiency two-level PSC converter with 10V input voltage. However, this increase would reduce a increase the power density and switching loss, respectively [10].

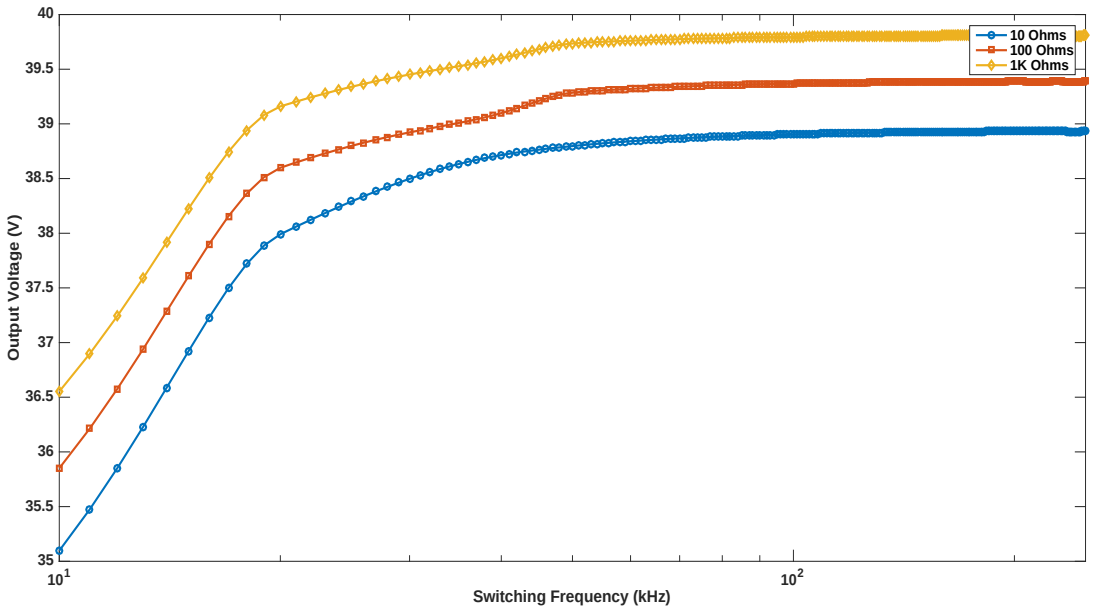


Figure 2.8: Switching frequency against the output voltage.

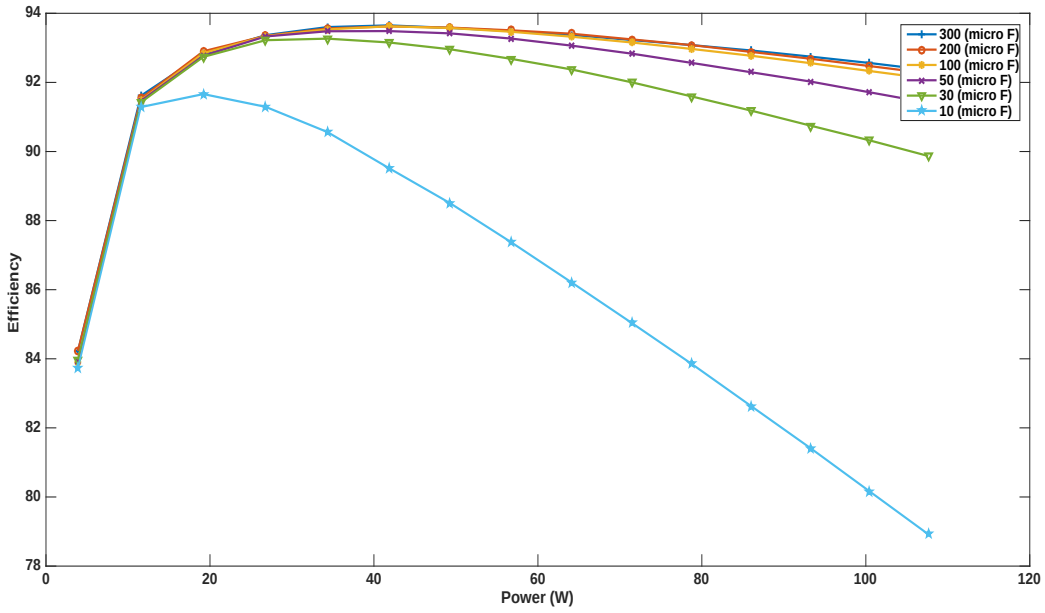


Figure 2.9: The 1-to-4 PSC efficiency at different capacitors' sizes.

2.4 Fast-switching limit impedance of the second order PSC converter

Another important parameter can be determined by analyzing the SC converter to find the fast switching limit (R_{Fsl}). Similar to $a_{c,i}$, each switch in the SC converter has a charge multiplier value that is represented as a_r.

$$a_r = [a_{r,s1}\ a_{r,s2}\ a_{r,s3}\ a_{r,s4}\ a_{r,s5} a_{r,s6}\ a_{r,s7}\ a_{r,s8}]^T \tag{2.27}$$

a_r charge multipliers of the eight switches of the 1-o-4 PSC converter are presented in (2.28),

$$a_r = [\,1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1]^T \tag{2.28}$$

The passing current trough of each switch is assumed to be constant. Since four modes of operation exist, the charge flow is multiplied by 4.

$$i_r = 4 q_r f_{sw} \tag{2.29}$$

The average power loss of each switch can be calculated by multiplying the total of the multiplication R_{ds_on} by (2.29). Due to the four modes of operation, P_{Fsl} is divided by 4

$$P_{Fsl} = \sum_{i=1}^{number\ of\ S} \frac{1}{4}(4a_{r,i}iout)^2 \tag{2.30}$$

$$R_{Fsl} = 4\sum_{i=1}^{number\ of\ S} R_{ds\_on}(a_{r,i})^2 \tag{2.31}$$

where $(a_{r,i})$ is the charge multiplier of eight switches in the 1-to-4 PSC converter.

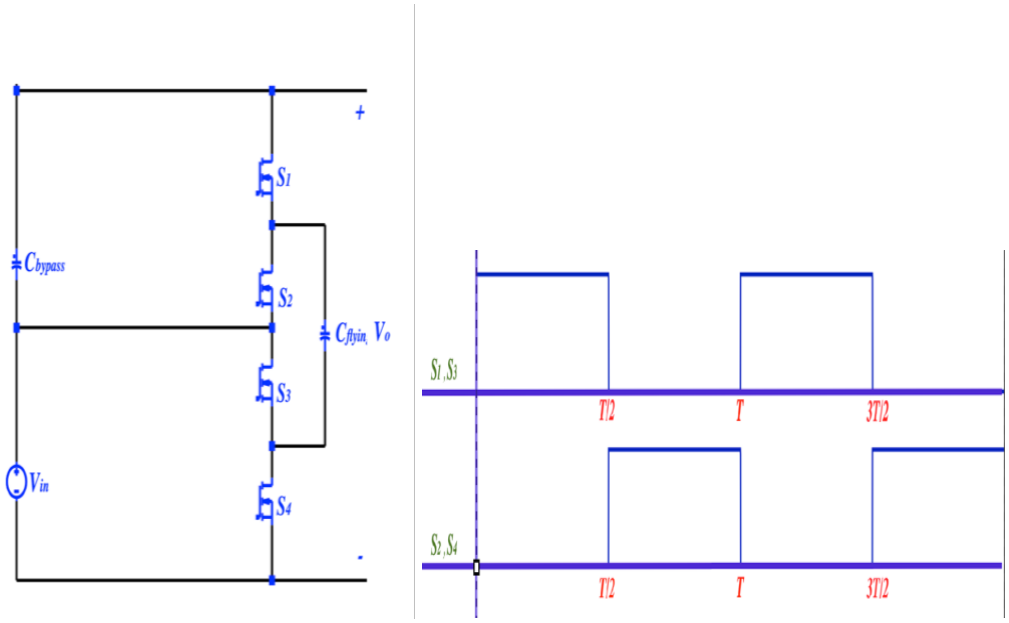
Elements	Equation
S_1, S_2, S_3, S_4	V_{in}
S_5, S_6, S_7, S_8	$2V_{in}$
C_1, C_2, C_{f1}	V_{in}
C_{f2}	$2V_{in}$

Table 2.3: Equation of the voltage stress on all semiconductors and capacitors.

2.5 Generalized power switched-capacitor converter

The proposed PSC converter contains one or more voltage doublers depending on the number of stages (Figure 2.10-a). Each cascaded voltage doubler is considered as a single stage of the PSC converter; for instance, three stages of PSC mean three voltage doublers are cascaded. Since each voltage doubler works to double the input voltage, each output voltage of a stage (voltage doubler) is the input voltage of a higher stage where the last stage will be connected to the output load. To generalize the PSC converter voltage gain, each additional stage (voltage doubler) is supplied by the output of the previous stage. Doubling each output of a certain stage concludes that the output voltage is a multiplication of the input voltage by 2^n where n is the number of stages. Each stage is controlled by

group signals that contain two control signals with a $\frac{T}{2}$ phase shift between them (Figure 2.10-b). For more than one stage, a phase shift is equal to $\frac{T}{2n}$ between any control group where n is the number of the stage. For example, if PSC has three stages, then three control groups are needed, and each group has two control signals. The first group is the reference, whereas $\frac{T}{4}$ and $\frac{T}{6}$ are phase shifts of the second and third groups, respectively.



(a) (b)

Figure 2.10: a) voltage doubler converter b) a generalized control diagram of the PSC converter.

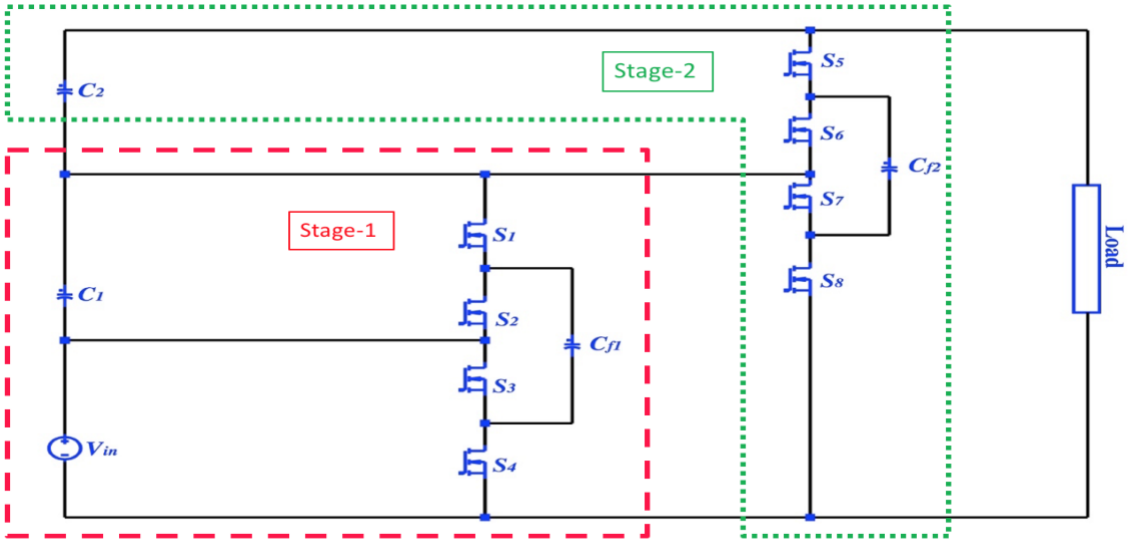


Figure 2.11: Two cascaded voltage doubler converters and formalized two stages of PSC converter.

2.6 A comparison between the proposed PSC converter with three SC converter topologies

The comparison between the proposed PSC and three known SC converter topologies covers the fundamental efficiency and output impedance. The proposed PSC converter successfully shows a privilege over the three other topologies in high efficiency achievement whereas a 1-to-4 ladder has the lowest efficiency as in Figure 2.13. In addition to that, the PSC converter successfully achieves SSL limit at a lower switching frequency faster than the other topologies as in Figure 2.14. In other words, the PSC converter requires less switching frequency to achieve a lower output impedance. A second lowest output impedance among the compared topologies, which is a series to parallel topology, means an additional comparison must be calculated between the PSC converter and 1-to-4 series to parallel the number of switches and the maximum voltage stress across the switches.

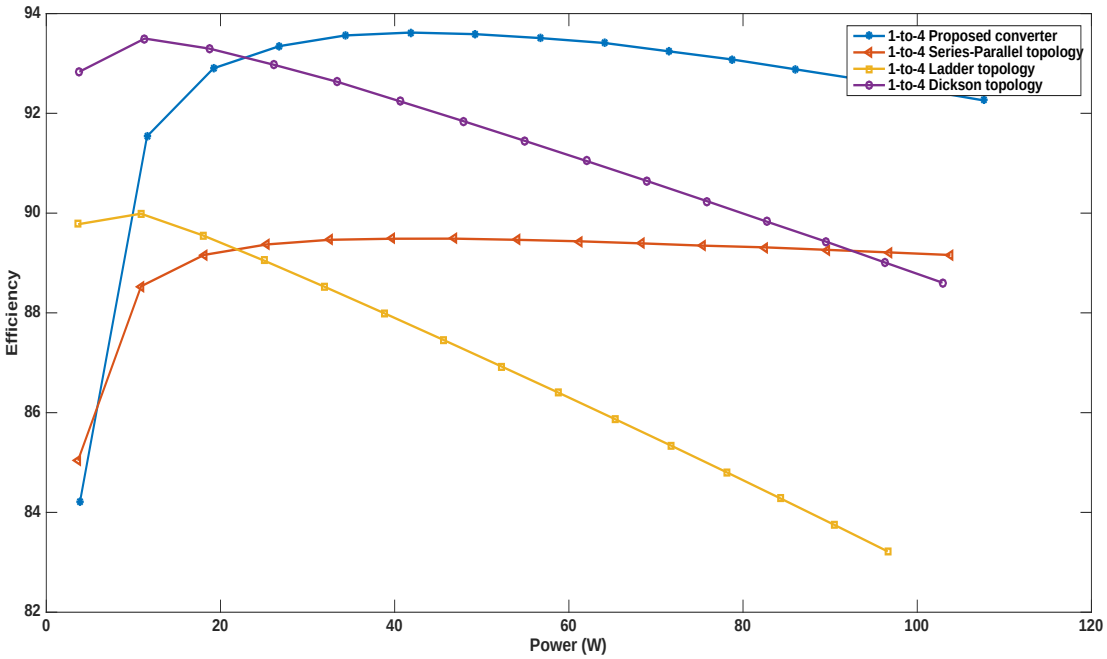


Figure 2.12: The efficiency of four compared topologies at different rated power.

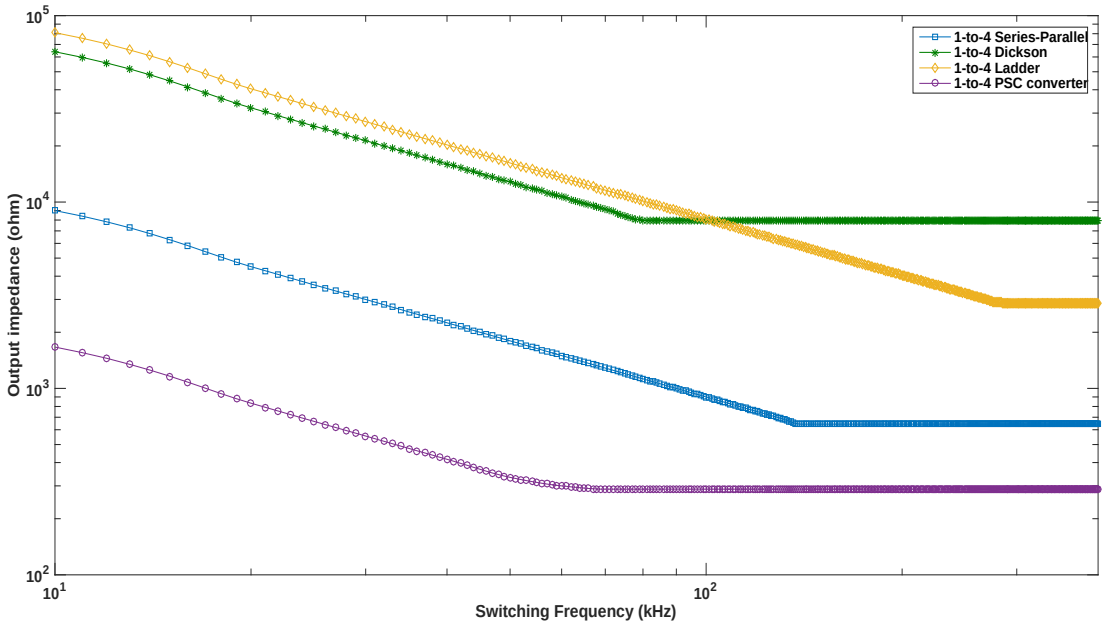


Figure 2.13: The output impedance of four compared topologies at different switching frequency.

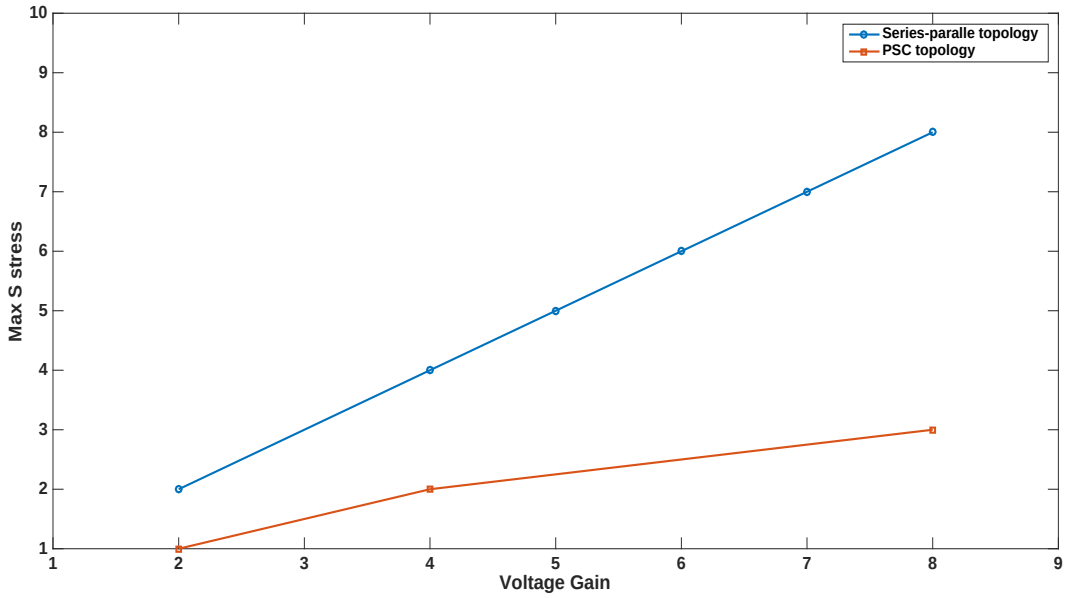


Figure 2.14: A comparison between PSC and series to parallel topologies in maximum stress on switches

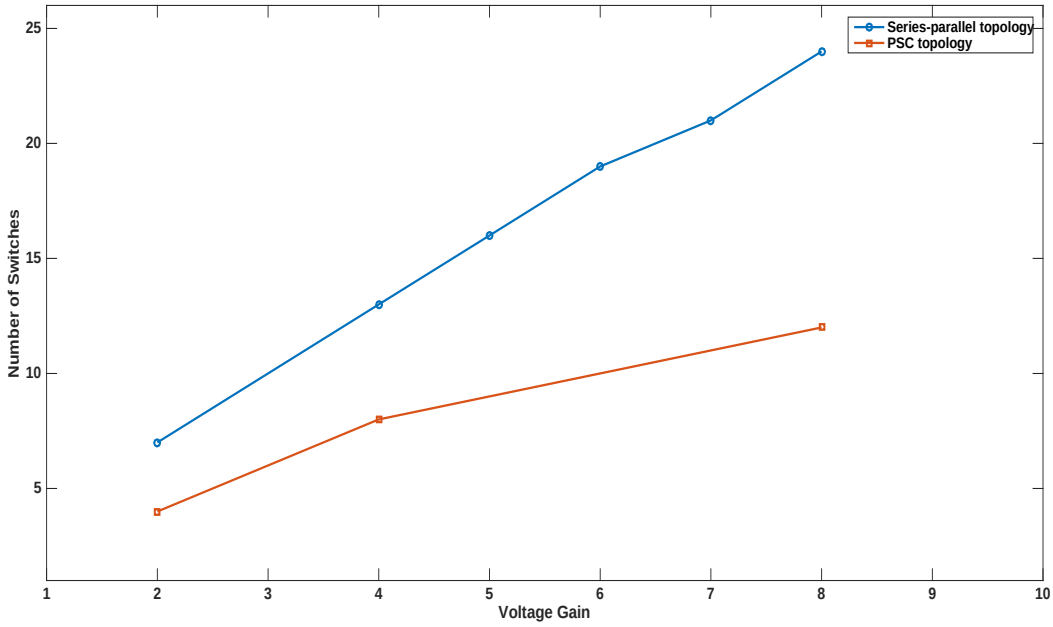


Figure 2.15: A comparison between PSC and series to parallel topologies in number of switches

CHAPTER THREE: AN INCOMPLETE SOFT-CHARGING OPERATION OF THE SECOND ORDER PSC CONVERTER

3.1 Introduction

The traditional technique to analyze a SC converter is known as a hard-charging operation where improving the output impedance depends on capacitors sizes and switching frequency. As an alternative technique of the hard-charging operation or the traditional technique, in this chapter the soft charging operation will be discussed. This technique is used to reduce the capacitors' sharing losses, improve their charging operation and reduce switching frequency requirement. To apply the soft-charging operation, a current load is placed as an output load. Across the current load, the voltage mismatch between capacitors and the input of the capacitors and the output is mostly presented. Charging and discharging capacitors losses which occur in the conventional SC converter (hard-charging) will be recovered by applying a soft-charging operation. Thus, resizing capacitors is possible and recommended. However, reducing capacitors' sizes causes a higher output voltage ripple which requires an insertion of an output LC filter to recover it. Moreover, a soft-charging operation helps to reduce the output impedance of the SC converter in its two limits, SSL and FSL. As mentioned in chapter 2, SSL limit is inversely proportional to switching frequency, thus the soft-charging operation helps to the SC converter achieve SSL limit at a lower switching frequency instead of a higher switching frequency as in hard-charging operation.

In this chapter an incomplete soft-charging operation of the proposed PSC converter will be discussed. Applying reduced voltage matrices of each operation mode and determining their null spaces are useful techniques to find the voltage change of each capacitor. The current transient and the voltage mismatch dispersions which are the essential benefits of the soft-charging technique are obtained for the second order of PSC converters. In addition to that, a reduction of the output impedance was determined by calculating its SSL limit [42-46].

3.2 An incomplete soft-charging operation of the second order PSC

To determine the flowing charge and the changing capacitors' voltage for the 1-to-4 PSC converter, we applied a KCL. Corresponding to the timing diagram in Figure 2.3-a, four operation modes are presented in Figure 2.3-b. The elements of each circuit in Figure 2.3-b, which are $V_{in}, V_{C_1}, V_{C_2}, V_{C_{f1}} V_{C_{f2}}$ and V_{out}, can be written in a voltage vector form.

$$V = [V_{in}\ V_{C_1}\ V_{C_2}\ V_{C_{f1}}\ V_{C_{f2}}\ V_{out}]^T \tag{3.1}$$

Each phase in Figure 2.3-b has four possible loops that can be expressed in a reduced matrix loop (3.3) [55]

$$A_i V^i = 0 \tag{3.2}$$

The reduced matrix's loops for the four modes can be written as in (3.3),

$$A_1 = \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ -1 & -1 & 0 & 0 & -1 & 1 \\ -1 & 0 & 0 & -1 & -1 & 1 \\ -1 & 0 & -1 & -1 & 0 & 1 \end{bmatrix}$$

$$A_2 = \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ -1 & -1 & 0 & 0 & 1 & 0 \\ 0 & -1 & -1 & -1 & 0 & 1 \\ 0 & 0 & -1 & 0 & -1 & 1 \end{bmatrix}$$

$$A_3 = \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ -1 & 0 & 0 & -1 & 1 & 0 \\ -1 & 0 & -1 & -1 & 0 & 1 \\ -1 & -1 & 0 & 0 & 1 & 0 \end{bmatrix} \tag{3.3}$$

$$A_4 = \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ 0 & -1 & -1 & -1 & 0 & 1 \\ 0 & -1 & 0 & -1 & -1 & 1 \\ -1 & -1 & 0 & 0 & -1 & 1 \end{bmatrix}$$

At the end of each mode, the voltage vectors become $\Delta V^i + V^i$

$$A_i\,(\Delta V^i + V^i) = 0 \tag{3.4}$$

where ΔV^i is the voltage change related to the load received charge. From (3.2) and (3.4), we have

$$A_i\,\Delta V^i = 0 \tag{3.5}$$

In the steady state assumption, the total voltage changes for the four operation modes equal zero.

$$\Delta V^1 + \Delta V^2 + \Delta V^3 + \Delta V^4 = 0 \tag{3.6}$$

since V_{in} is a constant DC source, then $\Delta V_{in} = 0$. To satisfy $\Delta V_{in} = 0$ a row with $[1 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0]$ is added to A_i

$$\Delta V^1 = a_1 W_1 + a_2 W_2$$

$$\Delta V^2 = b_1 U_1 + b_2 U_2$$

$$\Delta V^3 = c_1 H_1 + c_2 H_2$$

$$\Delta V^4 = d_1 X_1 + d_2 X_2 \qquad (3.7)$$

where $W_1, W_2\ U_1, U_2\ H_1, H_2, X_1, X_2$ are null spaces of the modified A_i matrices (after adding $[1 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0]$).

$$W = \left\{ \begin{bmatrix} 0 \\ 0.3541 \\ -0.5891 \\ 0.3541 \\ -0.5891 \\ -0.235 \end{bmatrix}, \begin{bmatrix} 0 \\ 0.4996 \\ 0.1673 \\ 0.4996 \\ 0.1673 \\ 0.6669 \end{bmatrix} \right\}$$

$$U = \left\{ \begin{bmatrix} 0 \\ 0.6295 \\ -0.3832 \\ 0 \\ 0.6295 \\ 0.2463 \end{bmatrix}, \begin{bmatrix} 0 \\ 0.0612 \\ 0.6732 \\ 0 \\ 0.0612 \\ 0.7344 \end{bmatrix} \right\}$$

$$H = \left\{ \begin{bmatrix} 0 \\ -0.1035 \\ -0.642 \\ -0.1035 \\ -0.1035 \\ -0.7455 \end{bmatrix}, \begin{bmatrix} 0 \\ 0.5244 \\ -0.3991 \\ 0.5244 \\ 0.5244 \\ 0.1253 \end{bmatrix} \right\}$$

$$X = \left\{ \begin{bmatrix} 0 \\ 0.6136 \\ -0.5569 \\ 0 \\ -0.5569 \\ 0.0566 \end{bmatrix}, \begin{bmatrix} 0 \\ 0.4728 \\ 0.2997 \\ 0 \\ 0.2997 \\ 0.7725 \end{bmatrix} \right\} \tag{3.8}$$

The voltage change ΔV^i can be calculated by

$$\Delta V^1 = a_1 W_1 + a_2 W_2$$

$$\Delta V^2 = b_1 U_1 + b_2 U_2$$

$$\Delta V^3 = c_1 H_1 + c_2 H_2$$

$$\Delta V^4 = d_1 X_1 + d_2 X_2 \tag{3.9}$$

where a_1, a_2, a_3, a_4, b_1, b_2, b_3 and, b_4 can be found by (3.10), and $\overline{W_1}$ $\overline{W_2}$ $\overline{U_1}$ $\overline{U_2}$ $\overline{H_1}$ $\overline{H_2}$ $\overline{X_1}$ $\overline{X_2}$ are the reduced form of $W_1, W_2\ U_1, U_2\ H_1, H_2, X_1,$ and X_2 (after eliminating the last row corresponding to ΔV_{out}). The ΔV_{out} is zero at an inductive load case.

$$[\overline{W_1} \quad \overline{W_2} \quad \overline{U_1} \quad \overline{U_2} \quad \overline{H_1} \quad \overline{H_2} \quad \overline{X_1} \quad \overline{X_2}] \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = 0 \tag{3.10}$$

$$\begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} -0.6794 \\ 0.3024 \\ -0.3050 \\ -0.1486 \\ 0.0837 \\ 0.1872 \\ 0.4934 \\ -0.215 \end{bmatrix} \tag{3.11}$$

Now (3.9) can be solved to calculate ΔV^i.

$$\Delta V^1 = \begin{bmatrix} 0 \\ -0.0895 \\ 0.4508 \\ -0.0895 \\ 0.4508 \\ 0.3613 \end{bmatrix} \Delta V^2 = \begin{bmatrix} 0 \\ -0.2011 \\ 0.0168 \\ 0 \\ -0.2011 \\ -0.1843 \end{bmatrix}$$

$$\Delta V^3 = \begin{bmatrix} 0 \\ -0.0895 \\ -0.1284 \\ 0.0895 \\ 0.0895 \\ -0.0389 \end{bmatrix} \Delta V^4 = \begin{bmatrix} 0 \\ 0.2011 \\ -0.3392 \\ 0 \\ -0.3392 \\ -0.1382 \end{bmatrix} \tag{3.12}$$

From (2.21) and (3.11) the capacitor sizes can be found by (3.13)

$$C_j = q_j / \Delta V_{Cj} \tag{3.13}$$

3.3 Slow-switching limit impedance (R_{ssl}) of second order PSC converter at a complete soft-charging operation

Similar to R_{ssl} calculation in section 2.3, the R_{ssl} of the PSC converter at soft-charging operation can be determine by using the following equation.

$$R_{ssl} = \frac{1}{6}\sum_{i=1}^{number\ of\ C} \frac{(a_{c,i})^2}{C_i\, fsw} \tag{3.14}$$

Where

$$\sum_{i=1}^{number\ of\ C}(a_{c,i})^2 = \frac{25}{18}$$

the voltage change ΔV_{Cj} of C_{f1} and C_{f2} is smaller than ΔV_{Cj} of C_1 and C_2, and as a result C_{f1} and C_{f2} need to be larger than C_1 and C_2. Thus, a reduction in C_1 and C_2 sizes reduces their voltage multipliers. This reduction in the total of capacitors' voltage multipliers results in a lower output impedance. A lower output impedance means a lower switching frequency is required to charge and discharge capacitors with maintained losses.

CHAPTER FOUR: A COMPLETE SOFT-CHARGING OPERATION OF THE SECOND ORDER PSC CONVERTER

4.1 Introduction

To achieve a complete soft-charging operation of any SC topologies, a split-phase control diagram is needed. The split phase diagram includes a dead time interval between any operation modes which are called transition modes. Moreover, instead of 50% duty cycle, some switches in the circuit operate in a duty cycle less than 50%. In their traditional operation, SC converters' capacitors are exiting and participating their charging and discharging processes in all conventional operation modes. In the split phase soft-charging operations, each transition mode at which some of the capacitors are isolated is considered. Capacitors' losses are mostly recovered by applying a complete soft-charging operation because of some capacitors' isolation. In this chapter, a split-phase control for the 1-to-4 PSC converter has been proposed.

4.2 A complete soft-charging operation of the second order PSC converter

The complete soft-charging analysis can be satisfied if and only if the Kirchhoff's voltage low (KVL) exists at all operation modes including the four transition modes. The control diagram in Figure 4.1-a allows eight modes of operation to exist as in Figure 4.1-b. Four of those modes are the same as the four modes of the conventional PSC converter

in Figure 2.3-b where the new four modes are basically the transition modes. The same procedures as applied for the incomplete soft-charging are repeated in this section. The A_i and B_i matrices Mode-1a, Mode-2a, Mode-3a, and Mode-4a are the same matrices as in Section 3.2. Since the extra four transition modes have three capacitors, only two KVL loops are possible for A_i matrices, which are presented as in following reduced loop.

$$A_{1b} = \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ -1 & 0 & -1 & -1 & 0 & 1 \end{bmatrix}$$

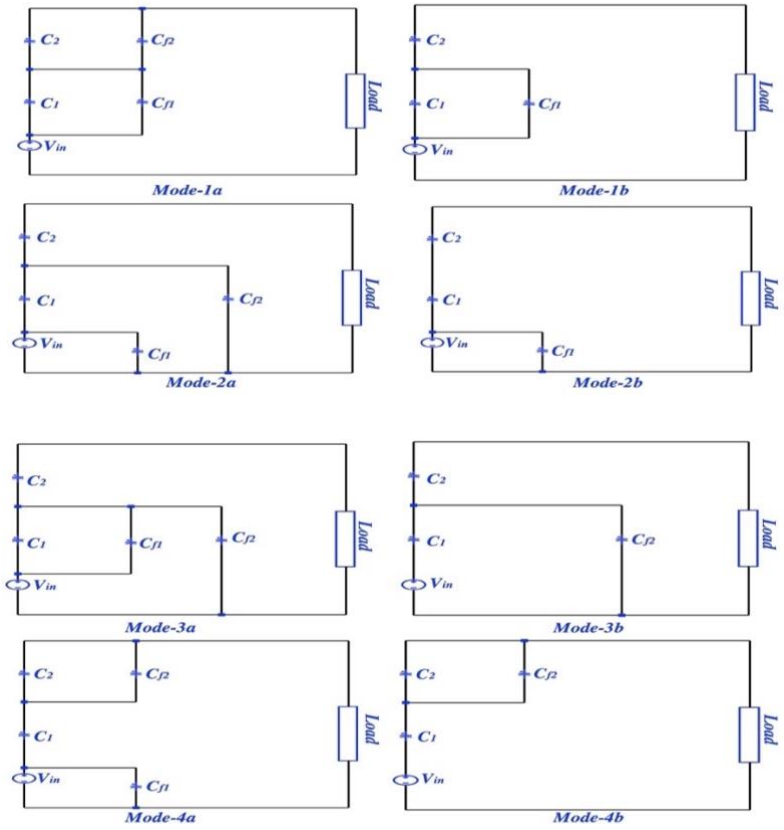
$$A_{2b} = \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ 0 & -1 & -1 & -1 & 0 & 1 \end{bmatrix}$$

$$A_{3b} = \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ -1 & -1 & 0 & 0 & 1 & 0 \end{bmatrix}$$

$$A_{4b} = \begin{bmatrix} -1 & -1 & -1 & 0 & 0 & 1 \\ -1 & -1 & 0 & 0 & -1 & 1 \end{bmatrix} \quad (4.1)$$

Although the transition modes contain three capacitors, their charge flow directions are the same as the charge flow direction of the basic modes as in Figure 2.7. However, the number of nodes in the transition modes is five instead of four due to the floating capacitor terminals. Since both terminals are floating, they are considered one node and expressed in an extra row in B_i. By using (2.17), the reduced matrices of the transition modes as in Figure 4.1 are presented as following (4.2).

(**a**)



(**b**)

Figure 4.1: (a) A proposed timing diagram to achieve a complete soft-charging in the 1-to-4 PSC converter; (b) eight operation modes of the 1-to-4 PSC converter in the complete soft-charging technique.

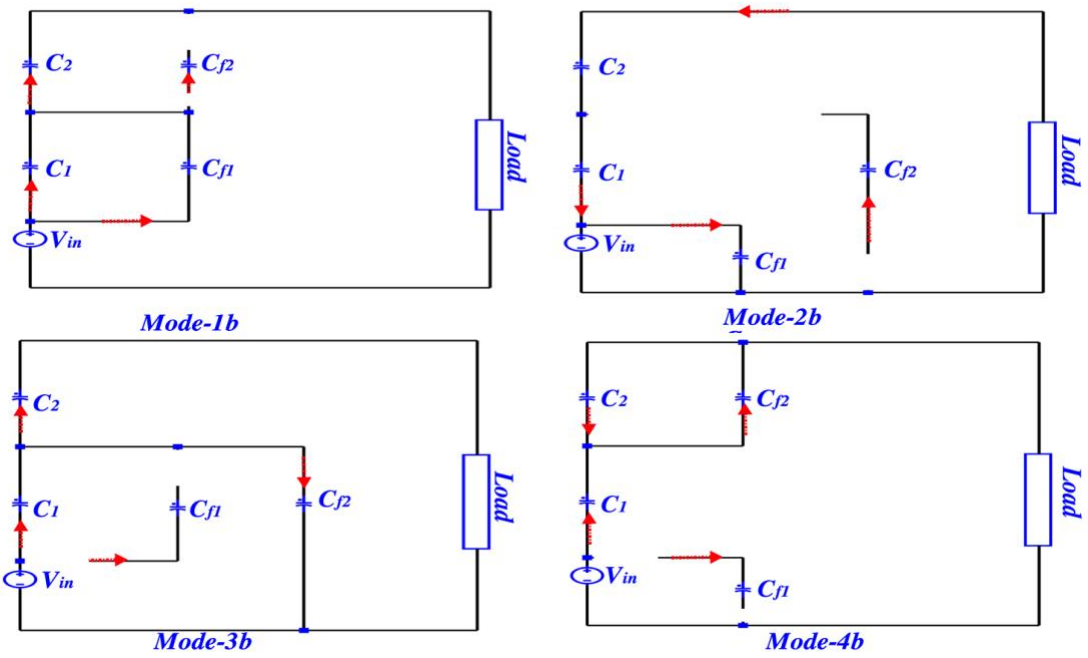


Figure 4.2: The charge flow for the split operation modes in the 1-to-4 PSC converter.

$$B_{1b} = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & 1 & -1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

$$B_{2b} = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & -1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

$$B_{3b} = \begin{bmatrix} -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}$$

$$B_{4b} = \begin{bmatrix} -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & -1 & -1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & -1 & 1 \\ 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \tag{4.2}$$

By applying the (2.17) the charge flow of the eight modes are the null space vectors of matrices B_i

$$q_c^{1,a} = \begin{bmatrix} 3 \\ 1 \\ 1 \\ 2 \\ 2 \\ 3 \end{bmatrix} q_c^{1,b} = \begin{bmatrix} 1 \\ -1 \\ 1 \\ 2 \\ 0 \\ 1 \end{bmatrix}$$

$$q_c^{2,a} = \begin{bmatrix} -3 \\ -1 \\ -1 \\ -2 \\ -2 \\ -1 \end{bmatrix} q_c^{2,b} = \begin{bmatrix} -1 \\ 1 \\ -1 \\ -2 \\ 0 \\ -1 \end{bmatrix}$$

$$q_c^{3,a} = \begin{bmatrix} 3 \\ 1 \\ 1 \\ 2 \\ 2 \\ 1 \end{bmatrix} q_c^{3,b} = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 0 \\ 2 \\ 1 \end{bmatrix}$$

$$q_c^{4,a} = \begin{bmatrix} -3 \\ -1 \\ -1 \\ -2 \\ -2 \\ -1 \end{bmatrix} q_c^{4,b} = \begin{bmatrix} -1 \\ -1 \\ -1 \\ 0 \\ -2 \\ -1 \end{bmatrix} \tag{4.3}$$

By using (2.21), (2.19) can be rewritten with respect to the output charge of the capacitors and the load similar to (2.22).

The last rows in (4.3) represent the delivered charge. The total input charge equals 16, which is the sum of the input charges for all eight modes (4.3). The duty cycle of each mode to achieve a complete soft-charging is calculated in (4.4). Each mode has a certain duty cycle where the sum of the modes' duty cycles completes one period of the proposed split-phase control in as Figure 4.1-a.

$$D_{1a} = D_{2a} = D_{3a} = D_{4a} = \frac{q_{input\_i}}{q_{input\_total}} = \frac{3}{16}$$

$$D_{1b} = D_{2b} = D_{3b} = D_{4b} = \frac{q_{input\_i}}{q_{input\_total}} = \frac{1}{16} \tag{4.4}$$

4.3. Generalized split-phase control diagram of the power switched-capacitors converter

The split-phase control diagram varies from a topology of other SC converters, so each SC topology operates in a specific control diagram to achieve its complete soft-charging operation. The two levels of the PSC converter have a control diagram presented in Figure 4.1-a, which controls all eight switches in the design. The proposed control diagram allows eight modes of operation to be presented. Four of those modes are similar to operation modes of the hard-charging operation, whereas the rest are their transition modes. The difference between the four operation modes of PSC converter in its conventional and complete soft-charging operations is they have different duty cycle. In the hard-charging operation all four modes have a duty cycle equals to $\frac{1}{4}$ where this duty cycle reduces to $\frac{3}{16}$ in the complete soft-charging operation. The rest of the duty cycle is

the transition modes which is equal $\frac{1}{16}$. In case only a single level of PSC converter is designed, there will be two modes of operation in the hard-charging operation whereas there will be four modes at its complete soft-charging operation. The duty cycle of the two modes is $\frac{1}{2}$ in the hard-charging operation where this duty cycle reduces to $\frac{3}{8}$ in the complete soft-charging. The duty cycle of the transition modes of the single stage PSC converter equals to $\frac{1}{8}$. To generalize the duty cycles of each operation modes at different levels of PSC, each traditional mode has a duty cycle equal to $\frac{3}{2^{(2+n)}}$ where it equals $\frac{1}{2^{(2+n)}}$ for the transition modes.

4.4. Slow-switching limit impedance (R_{ssl}) for split-phase operation

The total output charge with respect to the input charge can be found in (2.18)

$$q_{out,total} = q_{out}^{1,a} + q_{out}^{2,a} + q_{out}^{3,a} + q_{out}^{4,a} + q_{out}^{1,b} + q_{out}^{2,b} + q_{out}^{3,b} + q_{out}^{4,b} \quad (4.5)$$

The total output charge with respect to the input charge is

$$q_{out,total} = q_{in} + \frac{q_{in}}{3} + \frac{q_{in}}{3} + \frac{q_{in}}{3} + q_{in} + q_{in} + q_{in} + q_{in} = 6q_{in} \quad (4.6)$$

Similar to section 2.1, determining the $R_{ssl\_split\_phase}$ would go through the same process as in Chapter 2; however, in the split-phase technique, there are eight operation modes instead of four. By applying (2.15), the output charge multipliers of each mode can be found as following

$$(a_{out}^{1,a} + a_{out}^{2,a} + a_{out}^{3,a} + a_{out}^{4,a} + a_{out}^{1,b} + a_{out}^{2,b} + a_{out}^{3,b} + a_{out}^{4,b}) = \frac{5}{3} \quad (4.7)$$

$$\sum_{capacitors} V_{ci}a_i = a_{ci}^{1,a}V_{ci}^{1,a} + a_{ci}^{2,a}V_{ci}^{2,a} + a_{ci}^{3,a}V_{ci}^{3,a} + a_{ci}^{4,a}V_{ci}^{4,a} + a_{ci}^{1,b}V_{ci}^{1,b} + a_{ci}^{2,b}V_{ci}^{2,b} + a_{ci}^{3,b}V_{ci}^{3,b} + a_{ci}^{4,b}V_{ci}^{4,b} \quad (4.8)$$

Due to the periodic cycles,

$\Delta V^i = \left(V_{ci}^{1,a} - V_{ci}^{2,a}\right) = \left(V_{ci}^{3,a} = V_{ci}^{4,a}\right) = (V_{ci}^{1,b} - V_{ci}^{2,b}) = (V_{ci}^{3,b} = V_{ci}^{4,b})$ and

$(a_{ci} = a_{ci}^{1,a} = -a_{ci}^{2,a})$, $(a_{ci} = a_{ci}^{3,a} = -a_{ci}^{4,a})$, $(a_{ci} = a_{ci}^{1,b} = -a_{ci}^{2,b})$, and $(a_{ci} = a_{ci}^{3,b} = -a_{ci}^{4,b})$ are assumed. By rewriting (2.24), with respect to the complete soft-charging operation, the $R_{ssl\_split\_phase}$ is presented from (4.9) to (4.11)

$$\frac{5}{3}V_{out} + \sum_{capacitors} 4\Delta V^i q_i = 0 \quad (4.9)$$

Where the capacitors' voltage ripple is represented as $\Delta V^i = q_i/4C_i$, then by dividing by ${q_{out}}^2$ then

$$\frac{5V_{out}}{3q_{out}} + \sum_{i=1}^{number\ of\ C} \frac{(a_{c,i})^2}{4C_i\, fsw} = 0 \quad (4.10)$$

where $\frac{V_{out}}{q_{out}fsw} = R_{ssl}$

$$R_{ssl} = \frac{3}{20}\sum_{i=1}^{number\ of\ C} \frac{(a_{c,i})^2}{C_i\, fsw} \quad (4.11)$$

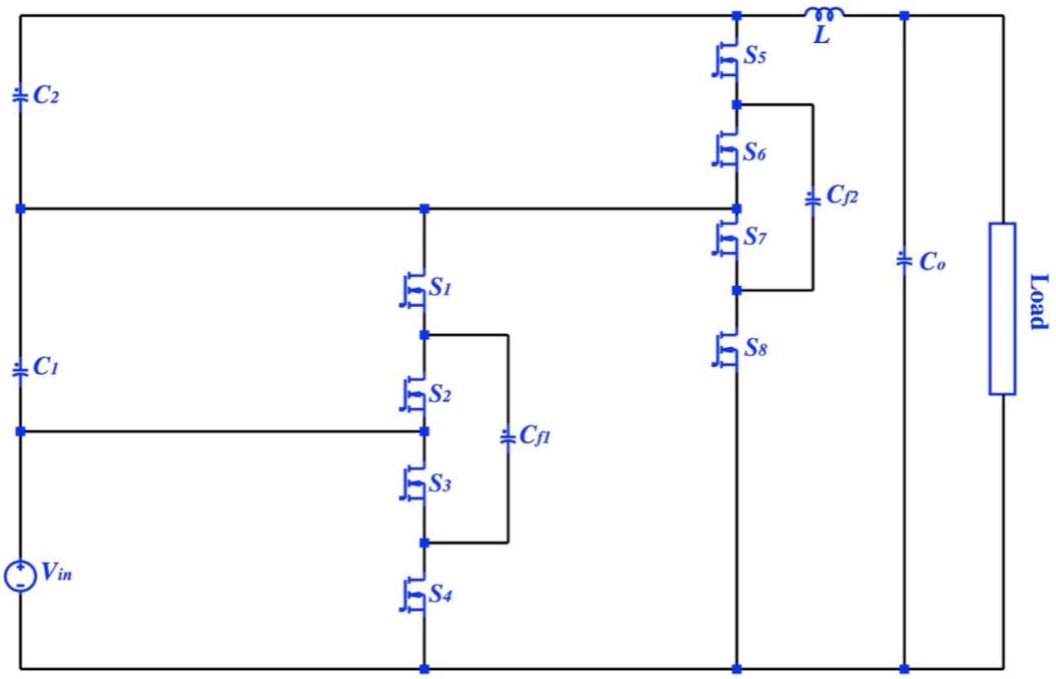


Figure 4.3: The 1-to-4 PSC topology with an output LC filter.

The complete soft-charging operation allows us to resize the capacitors; however, a small capacitor selection can result in a higher voltage ripple. To overcome the voltage's ripple, an output LC filter can be added to the output stage of the PSC converter. Figure 8 shows a 1-to-4 PSC with an output LC filter.

4.5. Simulated results of the second order PSC converter at three different operation techniques

The simulation design has been completed to determine the proposed split-phase control for the 1-to-4 PSC converter. The proposed split-phase control successfully supports the 1-to-4 PSC converter to achieve its complete soft-charging operation. Eight operation modes are approached in the following sequences: Mode 1-a, Mode 1-b, Mode 2-a, Mode 2-b, Mode 3-a, Mode 3-b, Mode 4-a, and Mode 4-b in the soft-charging

operation. However, only four operation modes were possible by controlling them conventionally, Figure 4.1. The scheme needs eight switches and four capacitors to rate a 40 V nominal output voltage with a supplied voltage of 10 V. Voltage stresses across the switches at either 0.25 V_{out} or 0.5 V_{out} . Due to the switches' stresses and the rated output voltage, all eight switches are selected to rate 40 V. Direct comparisons among four operation techniques—which are hard-charging, incomplete soft-charging, complete soft-charging-I and complete soft-charging-II—are presented in this section. In the hard-charging approach, C_1, C_2, C_{f1}, and C_{f2} are selected equally with a capacitance equal to 188 µF. Corresponding to (3.12), C_{f1} and C_{f2} have the lowest voltage change; C_1, and C_2 have the highest voltage change. Hence by using (3.13) C_1, C_2, C_{f1} and C_{f2} are selected differently (sections 3.2 and 4.2). In the incomplete soft-charging and complete soft-charging-I operations, C_1 and C_2 have a size equal to half of the C_{f1} and C_{f2} as in Table 4.1, which are 90 µF and 188 µF, respectively. Due to the switching dead time, the proposed split-phase control allows for more decrease of C_1, C_2, C_{f1} and C_{f2} sizes. The converter with reduced capacitors is referred to as a complete soft-charging-II in Table 2. Reducing the capacitor size results in a lower output impedance. Figure 4.4 shows the output impedance versus the switching frequency at hard-charging, incomplete soft-, and complete soft-charging-II. It can be clearly seen that the output impedance eventually decreases at a higher switching frequency selection.

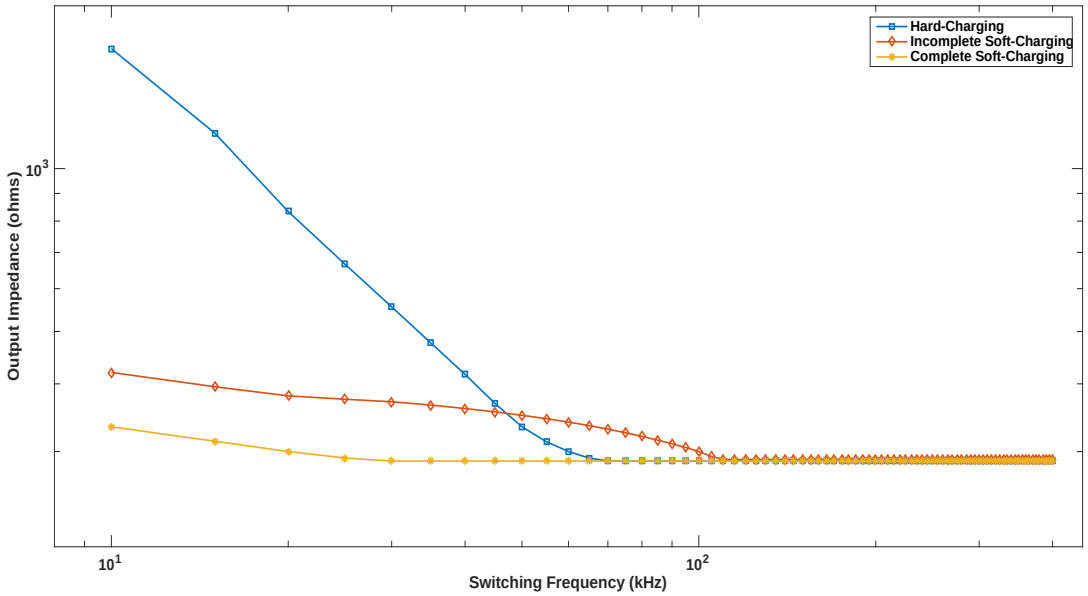


Figure 4.4: Simulation output impedance of the 1-to-4 PSC converter vs the switching frequency at three charging methods: hard-charging, incomplete soft-charging, complete soft-charging II.

However, unlike the hard-charging operation, applying the complete soft-charging-II technique keeps the output impedance almost constant at varied switching frequencies. Having an almost constant output impedance means the 1-to-4 PSC converter participates the FSL limits at a lower f_{sw}. Moreover, the split-phase control helps to eliminate the voltage mismatch between any two parallel capacitors. The voltage mismatch between $V_{Cf2} - V_{C2}$ and $V_{Cf2} - V_{in}$ has been recovered by applying split-phase control as in Figure 4.5 and Figure 4.6. In addition to eliminating the voltage mismatch, the complete soft-charging removes the current transient in the flying capacitors as in Figure 4.7.

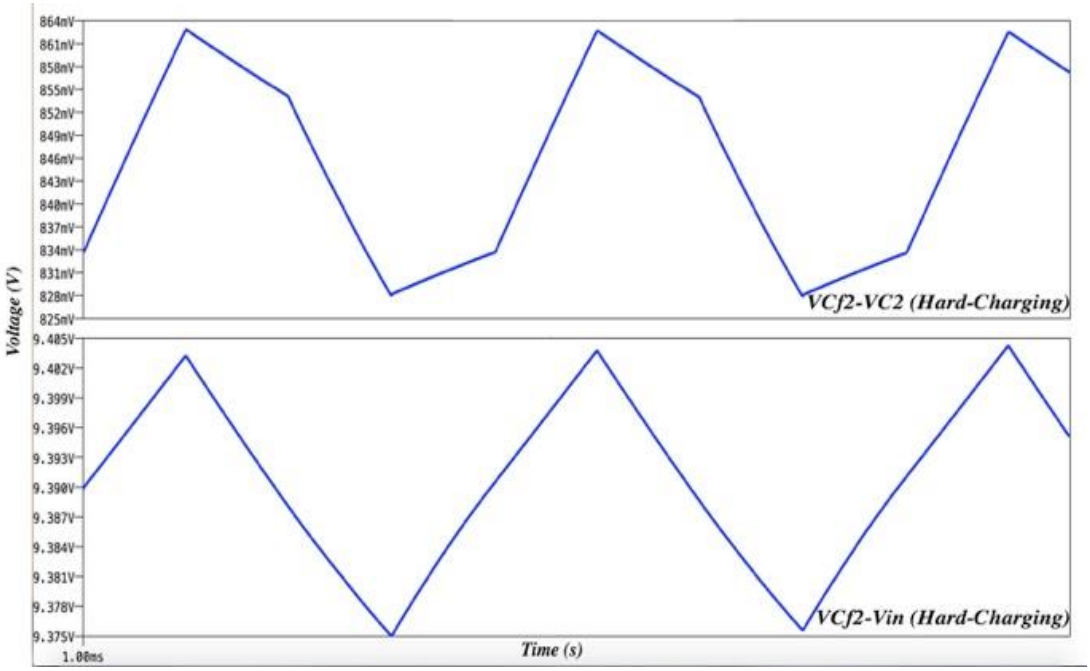


Figure 4.5: Capacitor voltage mismatch during hard-charging between $V_{Cf2} - V_{C2}$ and $V_{Cf2} - V_{in}$.

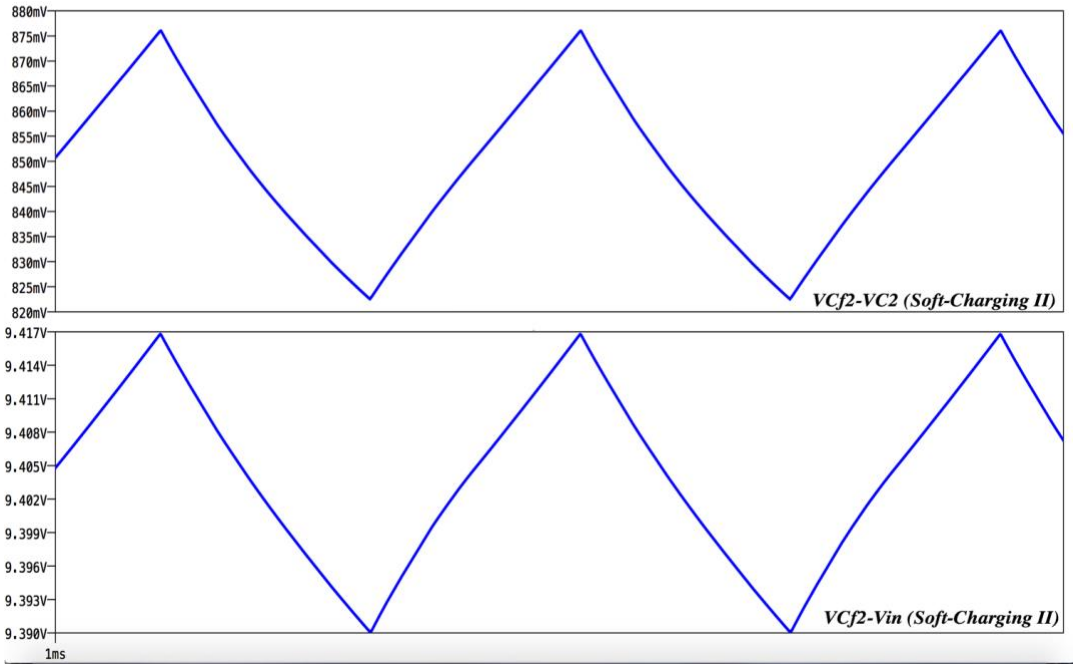


Figure 4.6: The elimination of the capacitor voltage mismatch during complete soft-charging II between $V_{Cf2} - V_{C2}$ and $V_{Cf2} - V_{in}$.

The decrease of the output impedance and the dead time switching should effectively recover the fundamental efficiency. However, reducing capacitor size causes an undesired higher output voltage ripple. To overcome the output voltage ripple, an output LC filter was added to the PSC converter as presented in Figure 4.3. (4.12), shows an equation to determine L where C is the equivalent capacitance in the 1-to-4 PSC converter [44][56].

$$f_{sw} \geq \frac{1}{2\pi\sqrt{LC}} \tag{4.12}$$

Figure 4.8 shows the 1-to-4 PSC efficiency against the I_{out} in four compared operations. The highest achieved efficiency occurs at the complete soft-charging-II with the LC filter insertion. Adding the LC filter could decrease the efficiency; however, this reduction is small compared to the high increase of the efficiency by using the soft-charging-II operation.

Parameter	**Value**
$\boldsymbol{V_{in}}$	10 V
$\boldsymbol{f_{sw}}$	200 KHz
$\boldsymbol{C_1, C_2, C_{f1} C_{f2,hard-charging}}$	188 µF
$\boldsymbol{C_{f1}, C_{f2}}_{\boldsymbol{complete\ soft-charging-I\ and\ incomplete\ soft-charging}}$	94 µF
$\boldsymbol{C_{f1}, C_{f2}}_{\boldsymbol{complete\ soft-charging-I\ and\ incomplete\ soft-charging}}$	188 µF
$\boldsymbol{C_1, C_2}_{\boldsymbol{-complete\ soft-charging-II}}$	20 µF
$\boldsymbol{C_{f1}, C_{f2}}_{\boldsymbol{-complete\ soft-charging-II}}$	40 µF
$\boldsymbol{C_{o-hard-charging}}$	200 µF
L of LC filter	50 nH

Table 4.1: Simulation parameters of PSC to operate in hard- and soft-charging

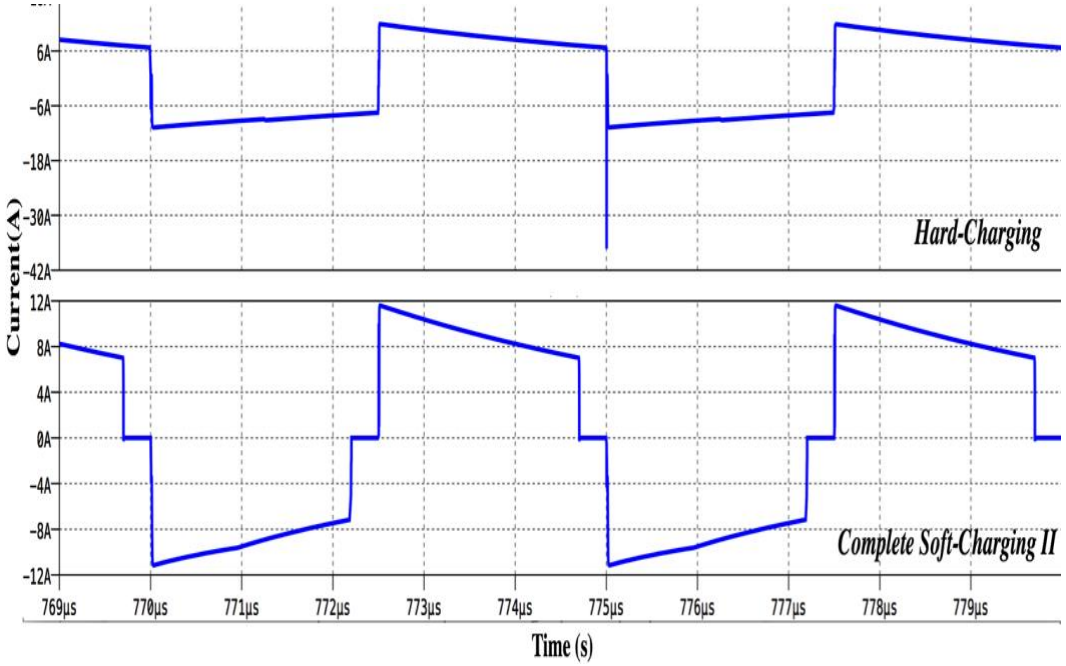


Figure 4.7: The current waveform of C_{f2} showing the transient in the hard-charging was eliminated by applying the complete soft-charging II.

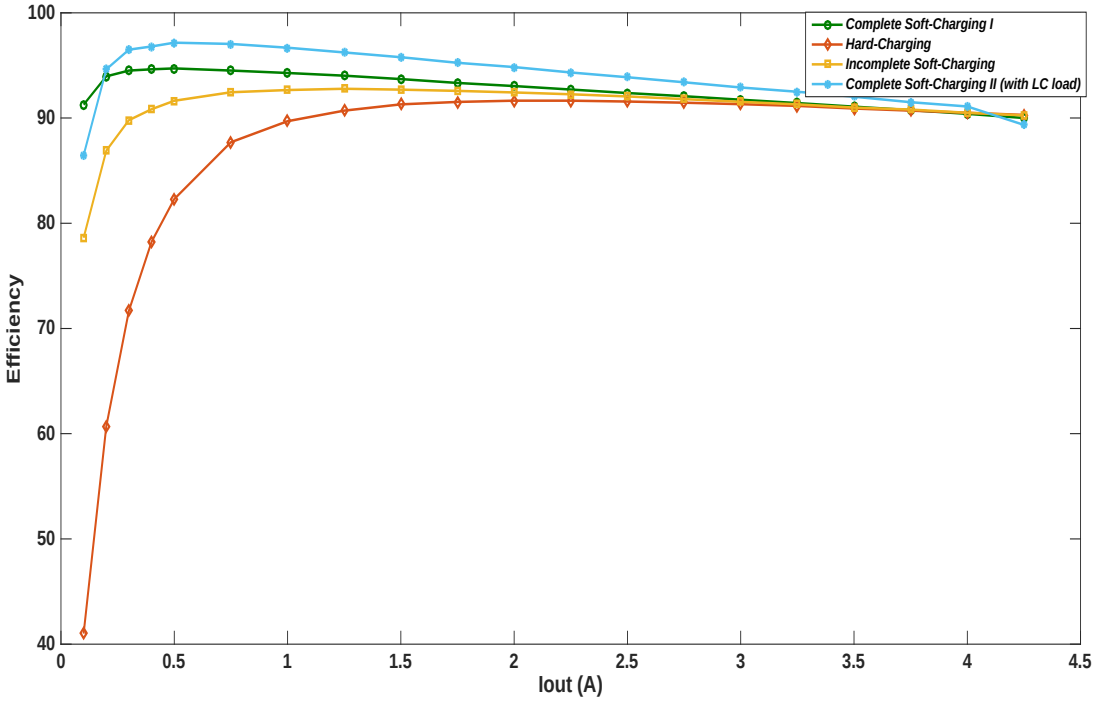


Figure 4.8: The PSC converter efficiency vs the rated power at different operation techniques: hard-charging, incomplete soft-charging, complete soft-charging I, and complete soft-charging II (with LC filter).

4.6 Numerical example

In this section a comparison between the hard-charging operation as in (2.27) and complete soft-charging operation as in (4.11) in R_{ssl} at three different causes

$$R_{ssl} = \frac{1}{6}\sum_{i=1}^{number\ of\ C} \frac{(a_{c,i})^2}{C_i\, fsw} \tag{2.27}$$

$$R_{ssl} = \frac{3}{20}\sum_{i=1}^{number\ of\ C} \frac{(a_{c,i})^2}{C_i\, fsw} \tag{4.11}$$

Where the total multipliers charge ($\sum_{i=1}^{number\ of\ C}(a_{c,i})^2$) at the hard-charging operation equals $\frac{5}{2}$ where it is $\frac{5}{18}$ for the proposed soft-charging operation.

Case I: C_i and fsw in (2.27) are equal C_i and fsw in (4.11) respectively.

Case II: C_i in (2.27) is equal C_i in (4.11) whereas fsw in (2.27) is double fsw in (4.11)

Case III: fsw in (2.27) is equal fsw in (4.11) whereas $C_i$in (2.27) is $4C_i$ in (4.11)

In case I, the soft-charging operation effectively deceases R_{ssl} at same values of C_i and fsw. The R_{ssl} at the soft-charging operation is only 10% of the R_{ssl} at the hard-charging operation where it is only 20% and 40 % in case II and case III respectively.

Charging operation	R_{ssl}	$(a_{c,i})^2$	**Same values of** $C_i\, fsw$
Hard-charging operation	$\frac{1}{6}\sum_{i=1}^{number\ of\ C}\frac{(a_{c,i})^2}{C_i\, fsw}$	$\frac{5}{2}$	1-Incomplete soft-charging operation (Case II) achieves (44.5% Reduction)
Incomplete soft-charging operation (Case I)	$\frac{1}{6}\sum_{i=1}^{number\ of\ C}\frac{(a_{c,i})^2}{C_i\, fsw}$	$\frac{25}{18}$	2-Complete soft-charging operation (Case II) achieves (88% Reduction)
Complete soft-charging operation (Case II)	$\frac{3}{20}\sum_{i=1}^{number\ of\ C}\frac{(a_{c,i})^2}{C_i\, fsw}$	$\frac{5}{18}$	

Table 4.2: A comparison among three charging operations in output impedance calculations.

4.7 A simulated result of two-level PSC by using EMTP-RV software and LTspice

To validate the simulated result of the second order PSC converter, the EMTP-RV simulator was used, and the results were compared with LTspice simulator results. The simulated parameters of the LTspice design and EMTP-RV are presented in Table 4.3. Both simulators show almost an exact output voltage at first and second order of the PSC converter as in Figure 4.9 . In addition to the output voltage comparison, a simulated efficiency comparison is presented in Figure 4.10. The hard-charging operation technique is the chosen operation technique at which the efficiency was calculated as in Figure 4.10. The elimination of the current transient is one of the advantages of applying the complete soft-charging operation. Figure 4.11 shows a current waveform of C_{f1} at hard-charging

operation. It clearly can be seen that the current waveform contains a transient which can be recovered by applying soft-charging operation Figure 4.12. Both LTspice and EMTP-RV software have proven the ability of complete soft-charging to eliminate the current transient.

Parameter	Value
V_{in}	10 V
f_{sw}	200 KHz
$C_{f1}C_{f2}$	188 µF
C_1C_2	94 µF
R_L	20
Switches	IPB075N04L

Table 4.3: Simulation parameters of LTspice and EMTP-RV simulators

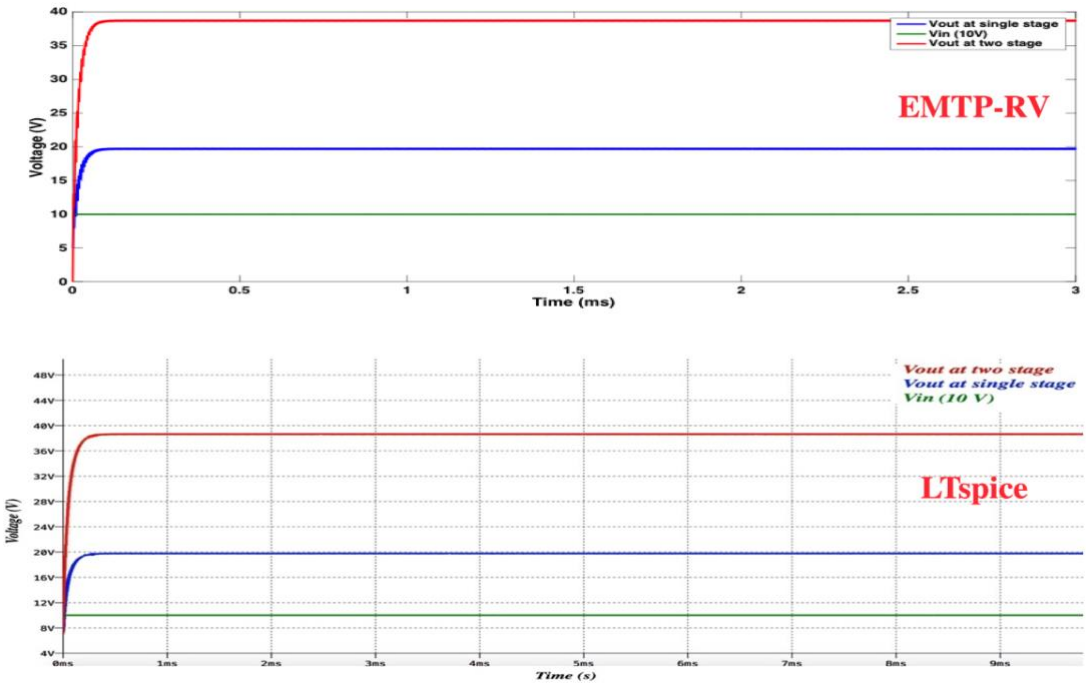


Figure 4.9: The input and output voltages of a 1-to-4 and 1-to-2 of the proposed PSC converter by using LTspice and EMTP-EV simulators.

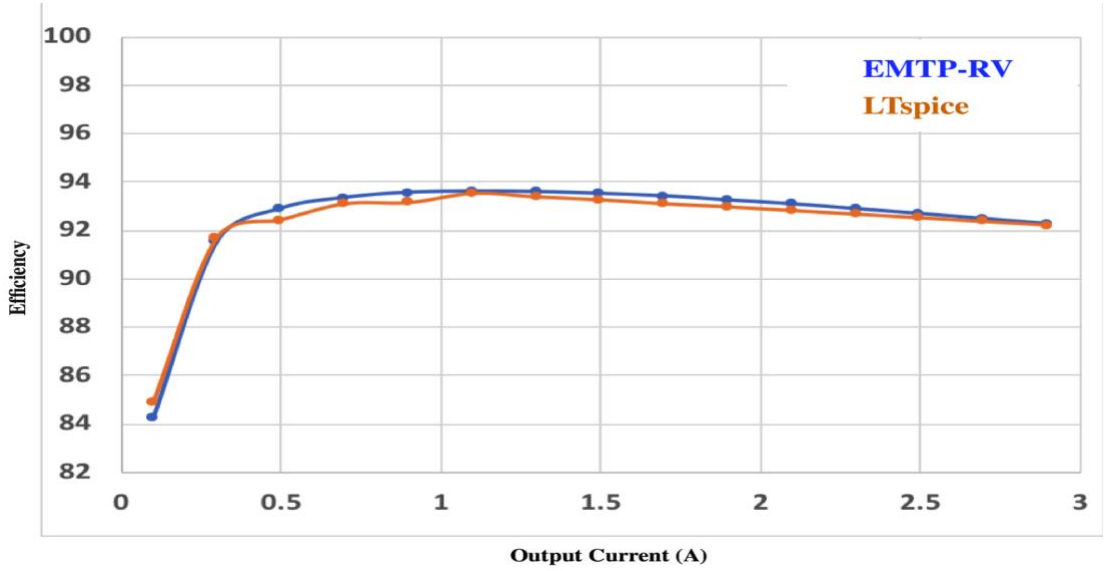


Figure 4.10: The efficiency of a 1-to-4 and 1-to-2 of the proposed PSC converter by using LTspice and EMTP-EV simulators.

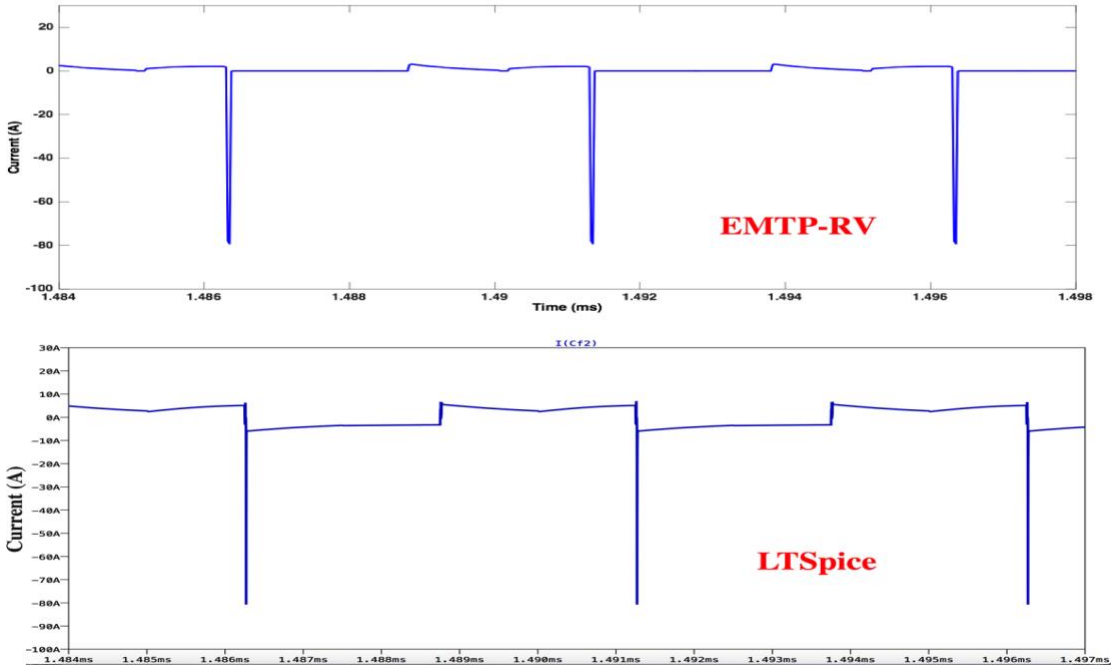


Figure 4.11: The current transient at C_{f2} hard-charging operation by using LTspice and EMTP-EV simulators.

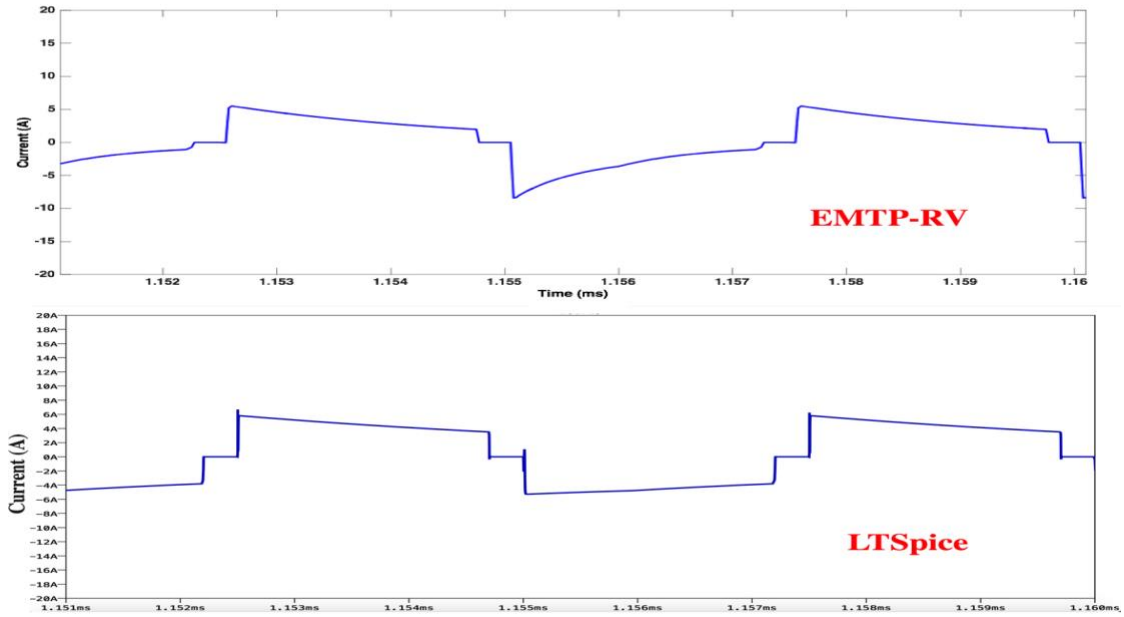


Figure 4.12: The current transient at C_{f2} is eliminated at complete soft-charging operation by using LTspice and EMTP-EV simulators.

CHAPTER FIVE: PSC CONVERTER APPLICATION FOR HIGH GAIN PROVISION

5.1 Introduction

Due to traditional gas resource limits, renewable energy has promised to meet the needs of the electricity demand. Sustainability goals related to renewable energy, such as wind energy and solar energy, encourage hundreds of research projects. However, since most renewable power produces low output, it has limited applications. For instance, photovoltaic cells usually produce an output voltage less than 24 V which could not power the usage of daily appliances. To expand renewable energy's application, DC-DC boost converters are recommended to optimize. The DC-DC boost converter is typically classified as either isolated or non-isolated. Inserting a power transformer into a DC-DC boost converter to form the isolated type increases the output voltage at a low duty cycle. Furthermore, having more than one switch in the isolated boost converter has been mentioned as a complicating aspect, and increasing voltage by using a non-isolated conventional boost converter is limited by switch voltage stress at a high duty cycle. Low voltage gain has also been marked as a dominant drawback of the conventional non-isolated converter. To increase the voltage gain of the DC-DC boost converter at a limited duty cycle, a multilevel boost converter (MBC) is recommended. The MBC works similarly to the conventional DC-DC boost converter; however, more than one output level

is added. The output levels (N) directly amplify the conversion ratio of the MBC at low duty cycle. The MBC builds up with a single inductor, a single switch, 2N-1 capacitors, 2N-1 diodes, and an output load [4][57-60]. Having such a high voltage conversion ratio with a non-isolated DC-DC voltage appears to be the most dominant advantage of MBC. Switch voltage stress has been regarded as an important parameter due to the switch singularity. Many studies have designed switched inductor models instead of input inductors to improve the conversion ratio [61-72]. However, most studies do not focus on the switch voltage stress as researchers aim to improve the voltage gain only as in [61-63]. However, some designs in addition to voltage gain improvement, they focus on maintaining the voltage stress of the switch [73-84]. In this chapter, a non-isolated switched inductor MBC achieves a high voltage conversion ratio and reduces the switch voltage stress. This work was successfully completed in a MATLAB/SIMULINK simulator, and the results were compared to two other MBC models, the first compared MBC has a single inductor as in [85-88] where the second MBC contains a switched-inductor with two inductors as in [89-91].

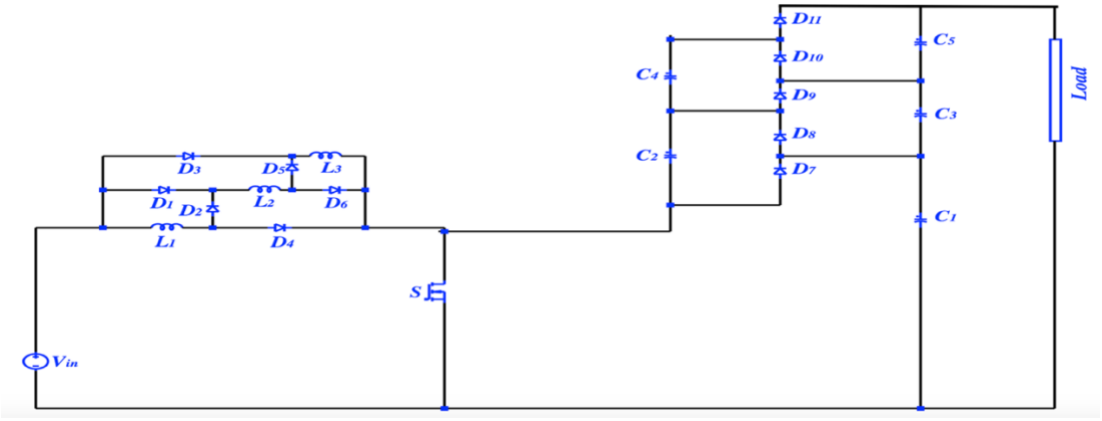


Figure 5.1: The MBC with the proposed switched inductor

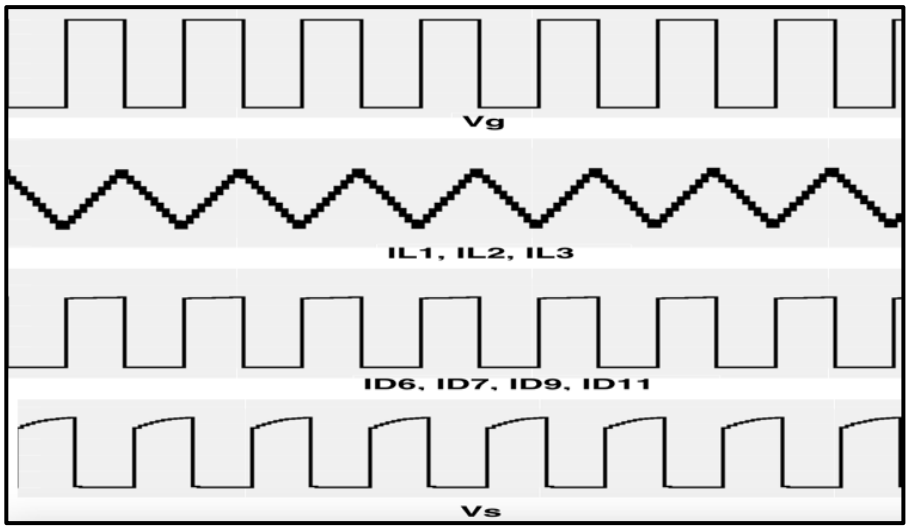


Figure 5.2: Steady state waveforms in CCM with L_1equal L_2 and L_3.

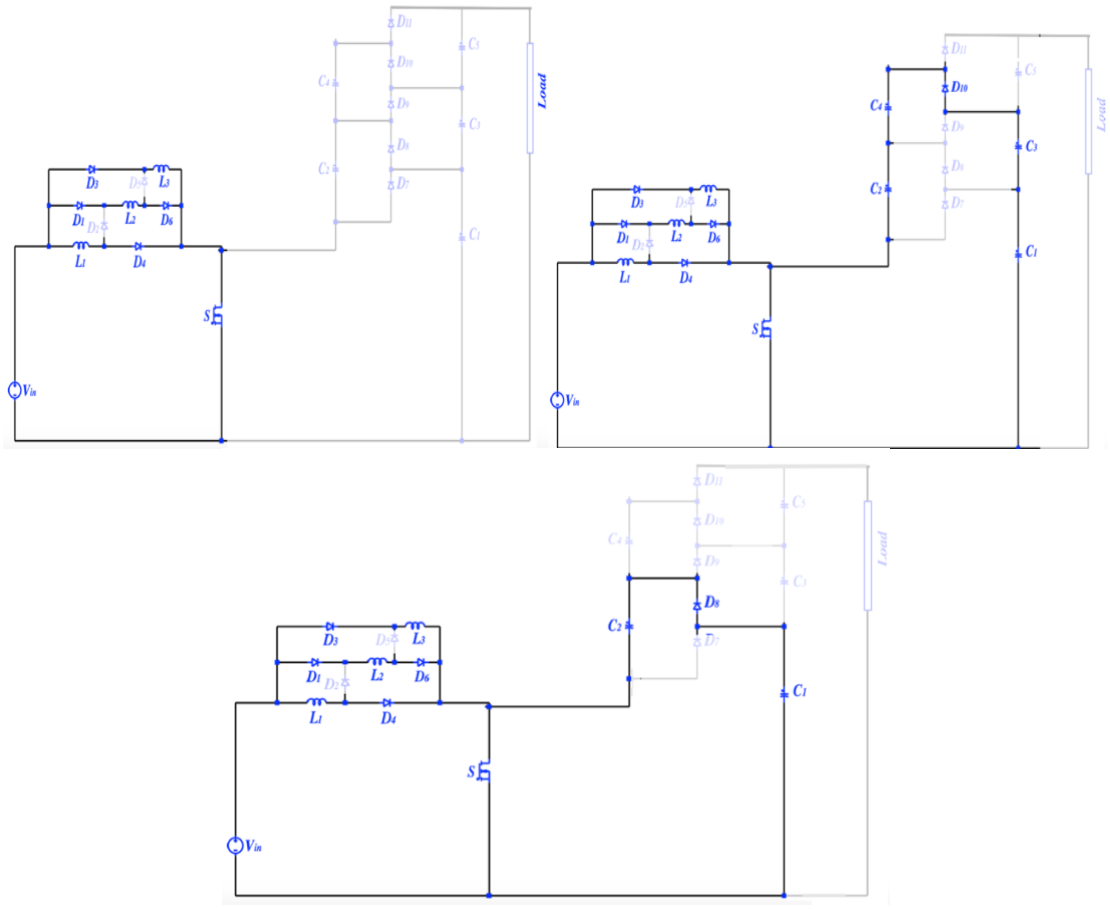


Figure 5.3: Mode 1 of the proposed three level MBC when S is on.

5.2 The proposed design MBC with switched inductor model

The proposed MBC is non-isolated with three levels (Figure 5.1). The design contains a 4N-1 diode, three inductors, 2N-1 capacitors, and a switch (*S*) which has been chosen to be a MOSFET. The output capacitors are connected parallel to the output load.

5.3 Modes of operation of MBC

Since the converter, which has one switch, operates in a continuous conduction mode (CCM) (Figure 5.2), two modes of operation are possible. The switch states form these two operation modes. The switch is on in Mode 1 and off in Mode 2.

5.3.1 Mode 1

During Mode 1, $L_1, L_2,$ and L_3 are charged by the input source V_{in} over D_6, D_7, D_9 and D_{11} (Figure. 5.3). Since C_1, C_3 and C_5 are assumed to be charged, then D_1, D_3 and D_5 are in an inverse biased state. Meanwhile, as L_1, L_2, L_3 are charged, D_2 is forward biased which permits C_1 to charge C_2. As C_1 charges C_2 to an equivalent voltage, D_2 shuts down and D_4 is activated. D_4 will remain on until voltage across C_1 and C_3 equals voltage across C_2 and C_4. This voltage distribution represents the end of the first mode.

5.3.2 Mode 2

In this mode, *S* is off, D_1, D_8 and D_{10} are on. Turning D_8 and D_{10} on initiates a series of connections between $L_1, L_2,$ and L_3 leading to discharge into C_1 through D_1. Once C_1 is fully charged, D_1 becomes reverse biased while D_3 becomes forward biased.

Once active, D_3 leads to charge C_3 until it is full. Since the voltage across C_1 and C_3 equals the voltage across C_2 and C_4, D_5 remains on until C_1, C_3 and C_5 are fully charged, marking the end of the second mode (Figure. 5.4).

5.4 Analysis of the proposed switched inductors boost converter

As previously mentioned, an MBC is simply a conventional boost converter with voltage multipliers added to its output. The three inductors L_1, L_2 and L_3 are assumed to be ideal. Since L_1, L_2 and L_3 have a parallel connection in Mode 1, they exhibit a voltage drop equal to V_{in} (5.1).

$$V_{in} = V_{L1} = V_{L2} = V_{L3} \tag{5.1}$$

$$I_c = \frac{-V_{out}}{R_L} \tag{5.2}$$

where V_{out} and R_L are the load voltage and resistor. In Mode 2, S is off and L_1, L_2 and L_3 have a series connection.

$$V_{in} = V_{L1} + V_{L2} + V_{L3} + V_{out} \tag{5.3}$$

since L_1, L_2 and L_3 are identical, they will be charged equally.

$$V_{in} = V_{L1} + V_{L2} + V_{L3} + V_{out} \tag{5.4}$$

$$3V_L = V_{L1} + V_{L2} + V_{L3} \tag{5.5}$$

rewrite (5.4) into (5.5) to get (5.6)

$$V_{in} = 3V_L + V_{out} \tag{5.6}$$

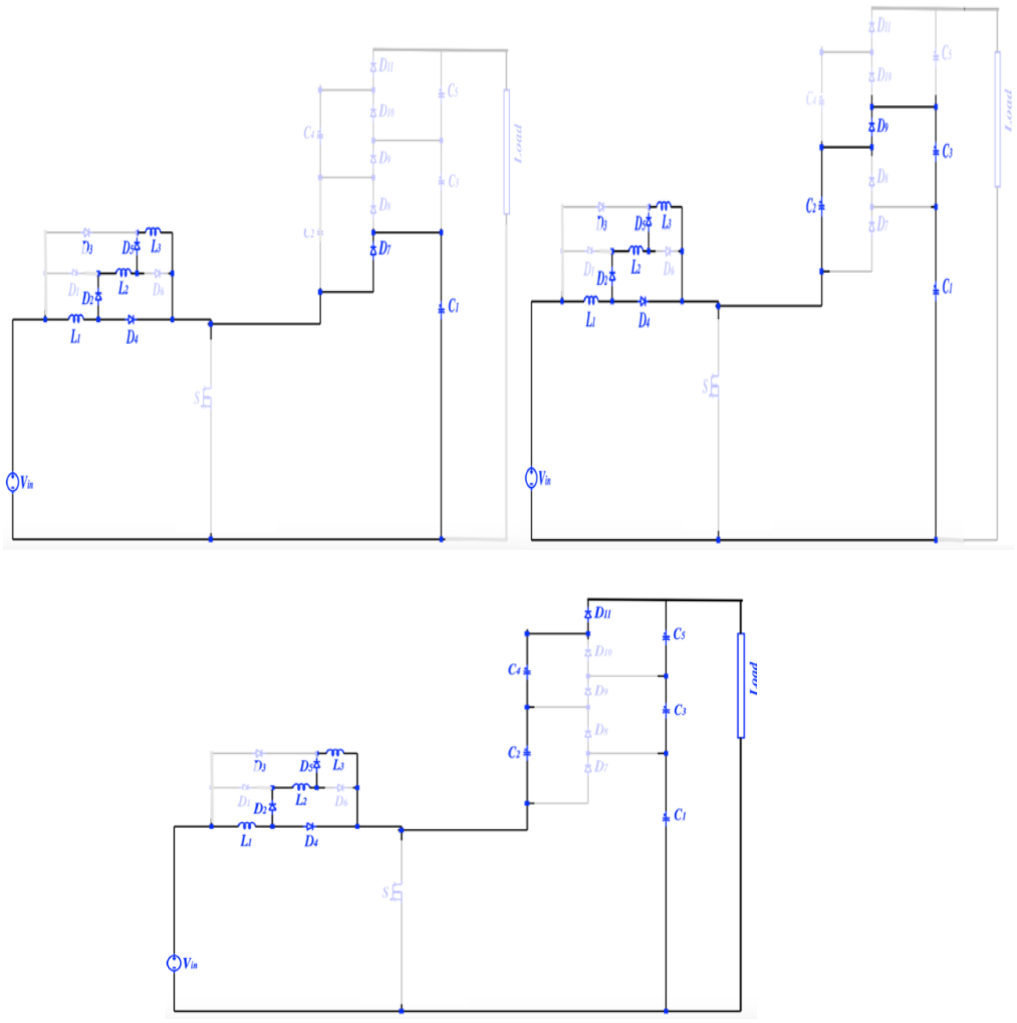


Figure 5.4: Mode 2 of the proposed three-level MBC when S is off

$$V_L = \frac{V_{in} - V_{out}}{3} \tag{5.7}$$

When applying the inductor voltage's second balance to (5.1) and (5.7) to conclude voltage gain of the proposed model,

$$DV_{in} = -(1 - D)\left(\frac{V_{in} - V_{out}}{3}\right) \tag{5.8}$$

by simplifying (5.8), converter gain in the conventional form equals

$$\frac{V_{out}}{V_{in}} = \frac{2D+1}{1-D} \tag{5.9}$$

To write the proposed converter in MBC form, multiple (5.9) by N [85]

$$\frac{V_{out}}{V_{in}} = \frac{N(2D+1)}{1-D} \tag{5.10}$$

where N is the number of the converter levels.

To calculate I_L which represents the total currents of $I_{L1},\ I_{L2}, and\ I_{L3}$,

$$P_{out} = P_{in} \tag{5.11}$$

(5.11) can be understood as (5.12)

$$I_{out}V_{out} = I_{in}V_{in} \tag{5.12}$$

where I_{in} is the input current of the boost converter

$$I_L=(\frac{V_{out}(2D+1)}{R_L(1-D)}) \tag{5.13}$$

MBC model in [85-88]	$\frac{V_{out}}{V_{in}} = \frac{N}{1-D}$
MBC model in [89-91]	$\frac{V_{out}}{V_{in}} = \frac{N(D+1)}{1-D}$
The proposed MBC	$\frac{V_{out}}{V_{in}} = \frac{N(2D+1)}{1-D}$

Table 5.1: Conversion ratio of three different MBC types at ideal components assumption.

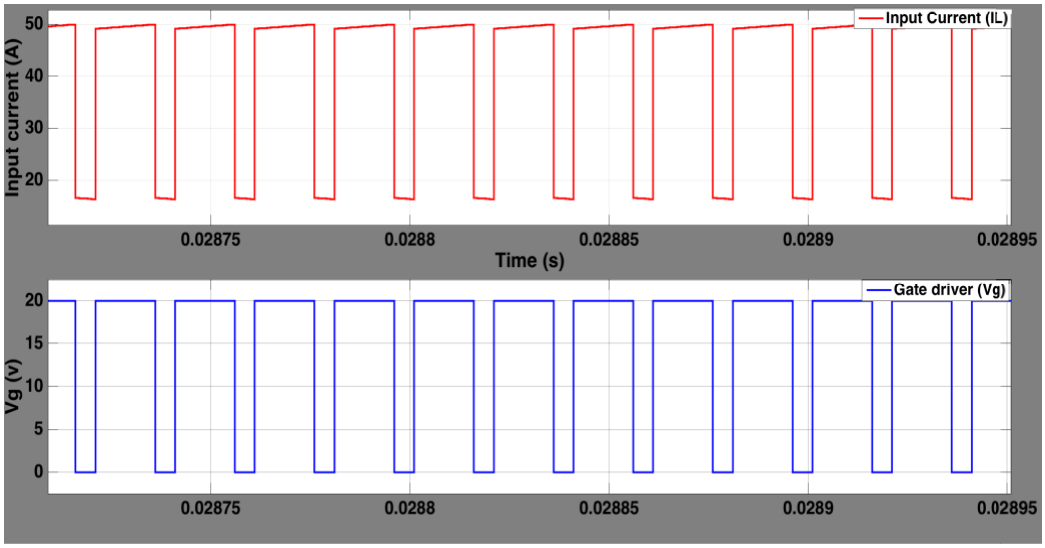


Figure 5.5: I_{in} with the duty cycle, shows L_1, L_2 and L_3 parallel and series connections.

Input Voltage (V)	12
Inductors ($L_1 = L_2 = L_3$)	1 mH
Capacitors	220 µF
Load	200 Ω
Duty Cycle	75%

Table 5.2: Design Parameters Calculated by [70]

5.5 A comparison between the proposed MBC and two other MBC topologies

The MATLAB SIMULINK software was used to study the principles of the proposed converter. The proposed MBC converter was compared to two similar MBC models as in [85-88] and [89-91]. The comparison among the three models was based on the voltage gain and the switch voltage stress. In [85-88] MBC was design with a single input inductor, where in [89-91] a switched inductor model was used instead of the input inductor. The suggested converter, which is supplied by 12V, has three voltage multipliers. The duty cycle was chosen to be 75% at a 50-kHz switching frequency ($\boldsymbol{f_{sw}}$). The operation of the MBC model's three input inductors includes a parallel connection in conduction mode where the inductors take a series connection in discharging mode as in Figure 5.5. In Figure 5.5 the total current of L_1, L_2 and L_3 which is I_{in} takes a pulse waveform that is similar to the gate drive signal (V_g). The identical phase between I_{in} and V_g suggests that a parallel and series connection of L_1, L_2 and L_3 in charging and discharging modes respectively is appropriate. Figure. 5.6 portrays the voltage gain versus the duty cycle of the three compared converters. The voltage gain is proportional to the duty cycle in any one of the three models; however, the highest value could be achieved when the proposed MBC is used. Figure 5.7 shows a relationship between the voltage gain and the switch voltage stress between 4 to 15 voltage gains of the three compared converters. The proposed converter has shown a tendency to reduce the switch voltage stress more effectively than the other two compared converters. Apart from the reduction on the switch voltage stress, the proposed converter successfully improves the voltage gain. Figure 5.8 represents the V_{out} of the three compared converters where the proposed converter outputs

280 V while [94-96] and [89-93] output 130 V and 210 V respectively. Figure 5.9 illustrates I_{out} which has the highest value when the proposed converter was used. In [85-88] and [89-91] I_{out} was found to be 0.7 and 1 A, respectively; however, it was recorded to be around 1.4 A of the novel model. The increase of I_{out} is a result of the voltage gain improvement. Since both V_{out} and I_{out} of the proposed model have shown increases, the converter rated power is increased as shown in Figure 5.10.

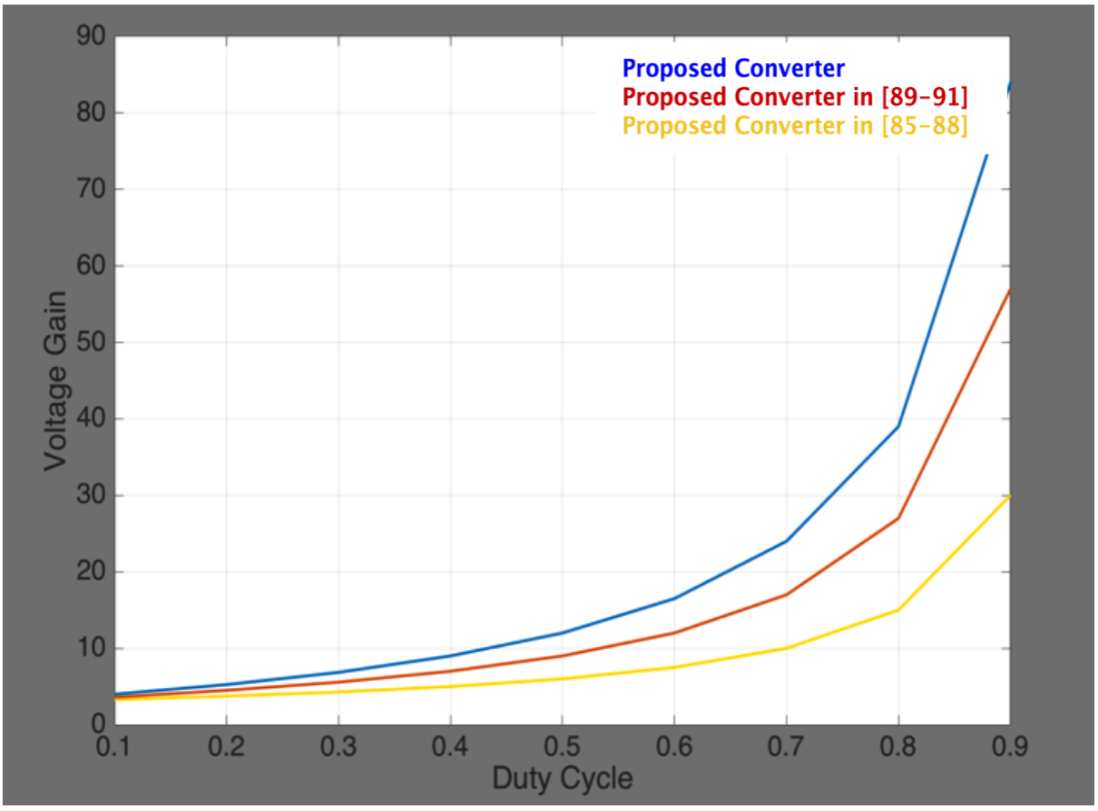


Figure 5.6: Duty cycle vs conversion ratio of the three MBC types

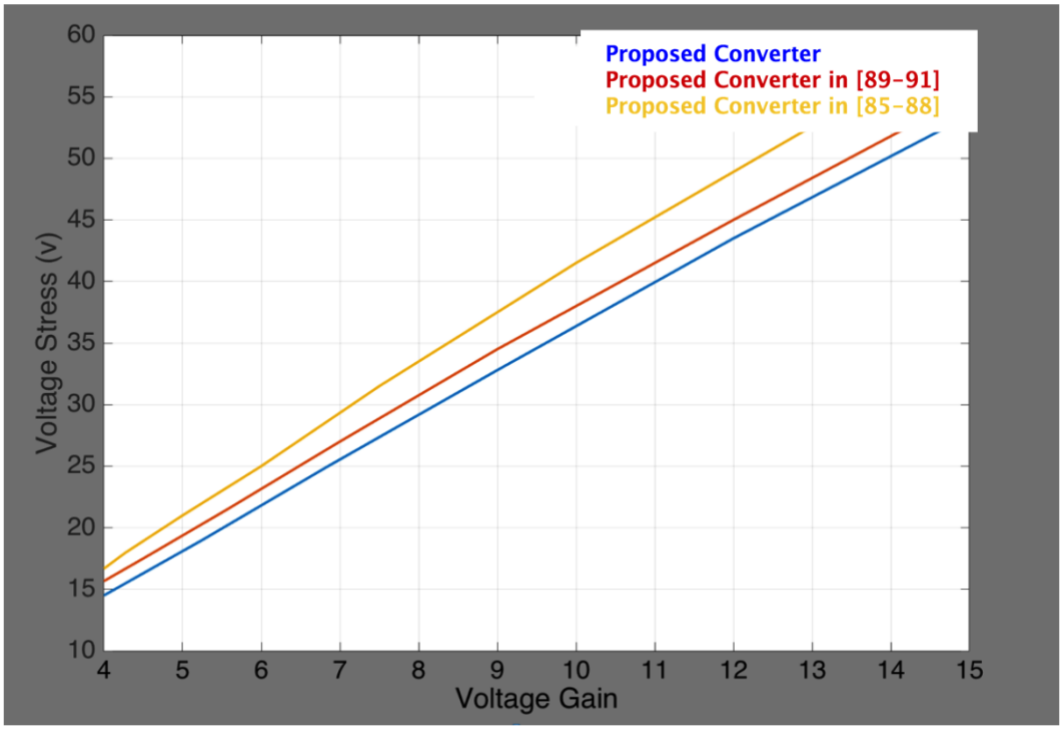


Figure 5.7: Switch voltage stress versus voltage gain of proposed converter and compared, [85- 88] and [89-91] between 4 to 15 voltage gains.

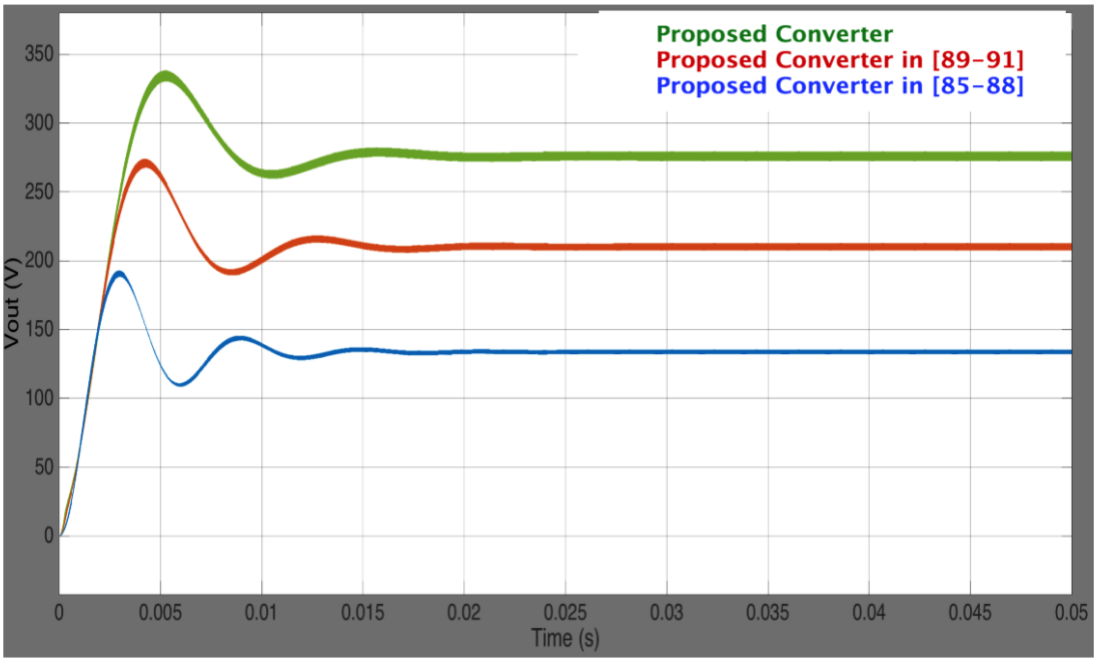


Figure 5.8: V_{out} of the three compared MBC types

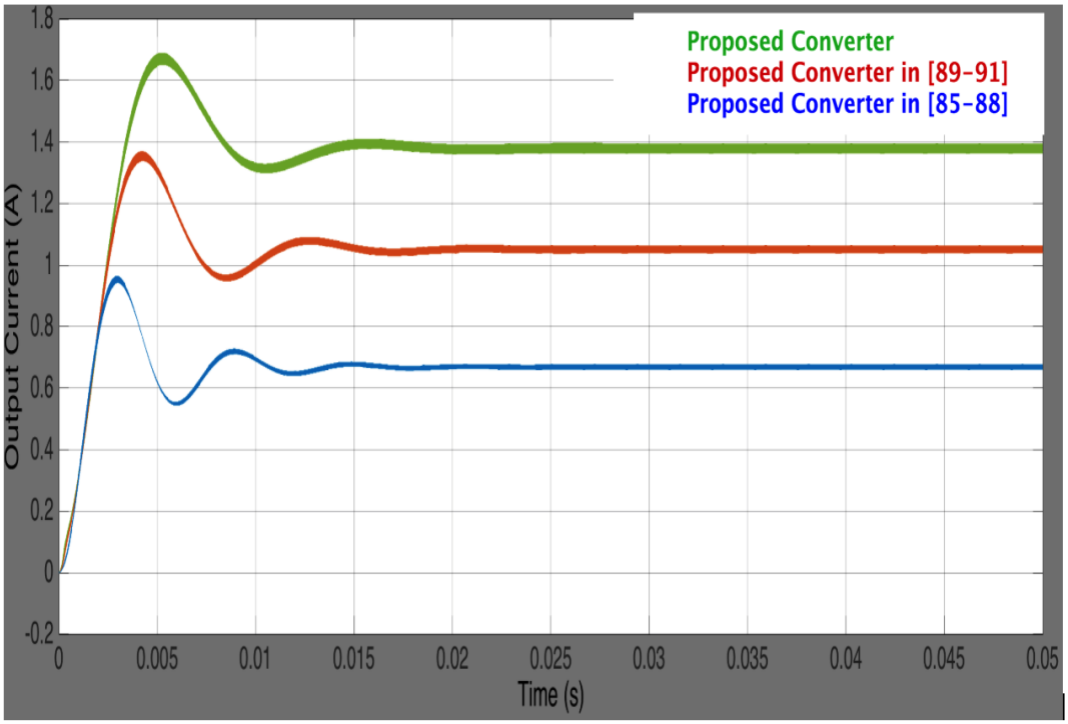


Figure 5.9: I_{out} of the three compared MBC types

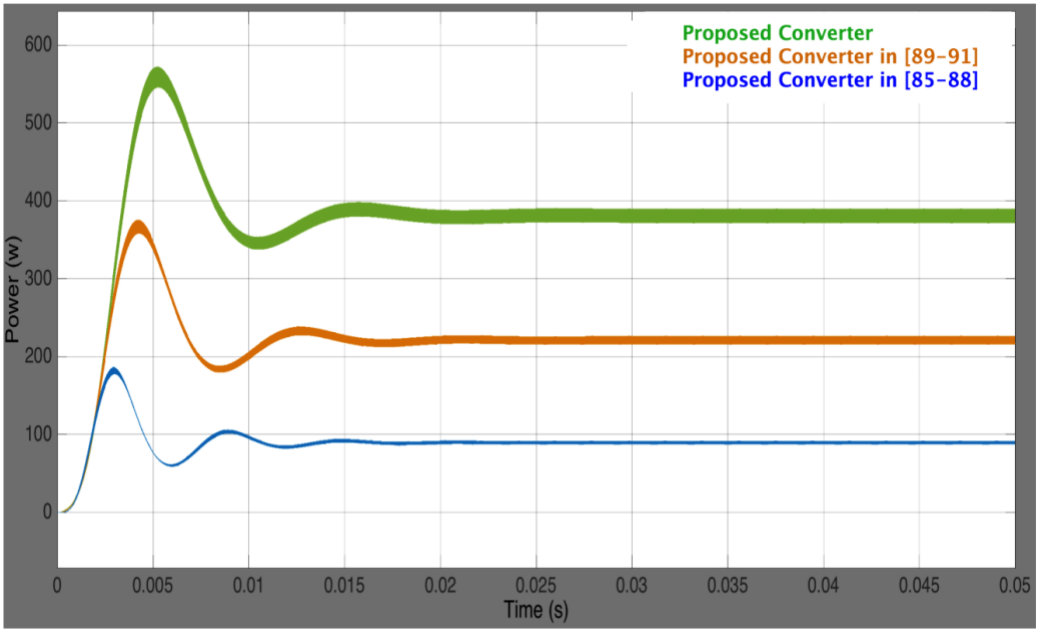


Figure 5.10: P_{out} of the three compared MBC types

5.6 Using a PSC converter as a voltage multiplier for a DC-to-DC switched-inductor boost converter

To meet the needs of electricity demand, renewable energy has promised to support traditional gas resources. Due to its sustainability goals, renewable energy, such as wind or solar power, inspire hundreds of research projects. The applications' limit of renewable power is related to a low power production which could not power the daily usage of appliances. Expanding renewable energy's application can be completed by DC-to-DC boost converters, which step up the renewable output power.

Isolated or non-isolated are two types that categorize DC-to-DC boost converters. The isolated boost converter category has a power transformer that divides the DC-to-DC boost converter into primary and secondary sides. The power transformer's insertion aims to increase the voltage gain; however, it could cause an electromagnetic interference. Furthermore, the power transformer reduces the power density due to its bulky size. As an alternative substitution of the isolated DC-DC boost converter is a non-isolated conventional boost converter. The non-isolated boost converter steps up the voltage by controlling the switch at a specified duty cycle. The duty cycle is proportionally related to the voltage gain; however, it is limited by switch voltage stress. As a result, a voltage gain's limit has been marked as a major drawback of the conventional non-isolated boost converter. To increase the voltage gain, adding a voltage multiplier to the output of the DC-to-DC boost converter, which is known as a multilevel boost converter (MBC), is recommended. Unlike to the conventional DC-to-DC boost converter, the MBC helps to amplify the conversion ratio at a low duty cycle. A single inductor, a single switch, 2N-1

capacitors, 2N-1 diodes, and an output load are the required components for designing the MBC.

On the other hand, the MBC is not ideal or without issues. For instance, the MBC fails to achieve the actual regulated voltage at a high duty cycle. The reason for that is having a high duty cycle means a low charging time; as a result, the output capacitors could not charge completely. Moreover, adding more diodes to increase the voltage gain could affect the fundamental efficiency. In this chapter, we have cascaded the proposed power switched-capacitor converter (PSC) [27-28] to a boost converter. The proposed converter (PSC-boost) works similarly to the MBC; however, the switched capacitors or voltage multipliers are located in the input source. Using SC cells has proven a strength to improve the voltage gain of the boost converter [91-96]. Furthermore, instead of using uncontrollable switches (diodes), the PSC-boost contains fully controllable switches (MOSFET) to complete the output capacitors' charging and discharging processes. Choosing switches instead of diodes might increase the cost however, that would expand the boost converter applications. For instance, instead of using a boost converter for low power application, it can be suitable for high power application such as PV system. A switched inductor model proposed in [97] has been used instead of the boost side's inductor. The PSC-boost shows the ability to achieve a high voltage gain at a high duty cycle. In addition to the high gain achievement, the PSC-boost is more efficient than the MBC converter. The MA TLAB/SIMULINK simulator was used to successfully complete the results of this section.

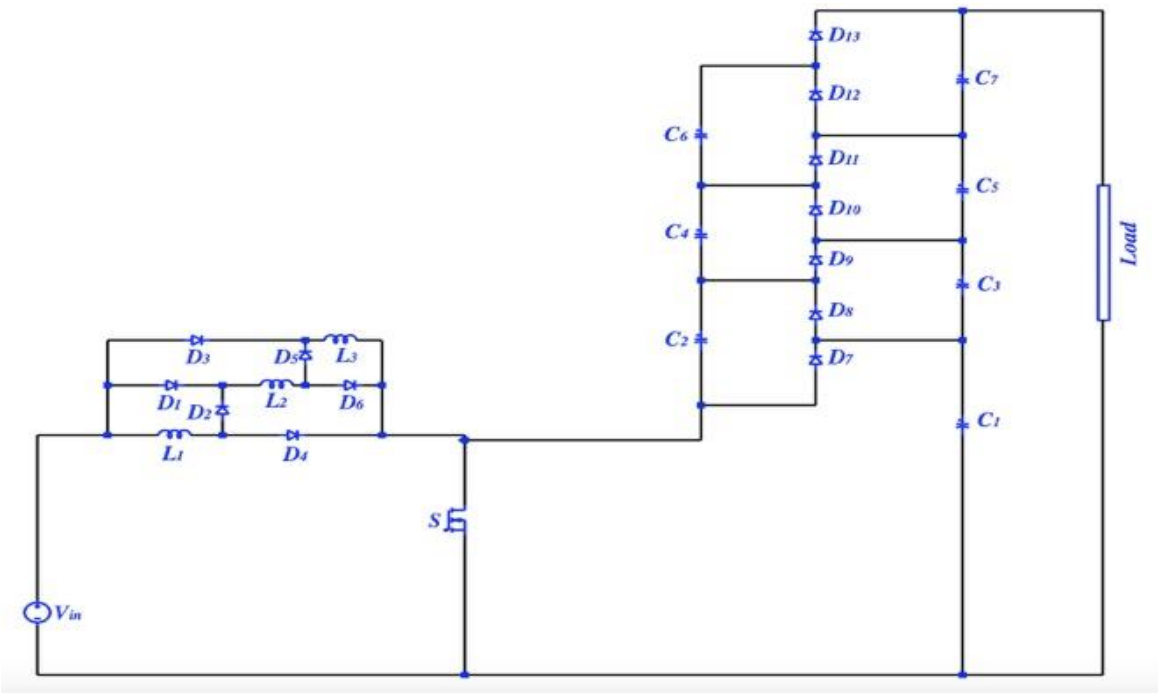


Figure 5.11: The 4-level MBC converter:

5.7 Analysis of the proposed switched inductors model by using PSC cells as voltage multipliers

The proposed PSC-boost converter is simply a PSC switched-capacitor converter that cascaded to a non-isolated boost converter. Similar to the MBC converter, the proposed model contains capacitors' multiplier cells. Using either diodes or MOSFETs allows capacitors of the multiplier cells to charge and discharge. To control capacitors' charging and discharging process, diodes are used in the MBC while MOSFETs are used in the PSC-boost converter [98][99]. The multiplier cells in the MBC converter are connected to the output side of the conventional boost converter whereas they are connected to its input side in the PSC-boost converter. In the PSC-converter, a switched inductor model that proposed in [97] is inserted instead of the single inductor. The PSC-boost contains five switches, five capacitors, seven diodes, and three inductors (Figure 5.12).

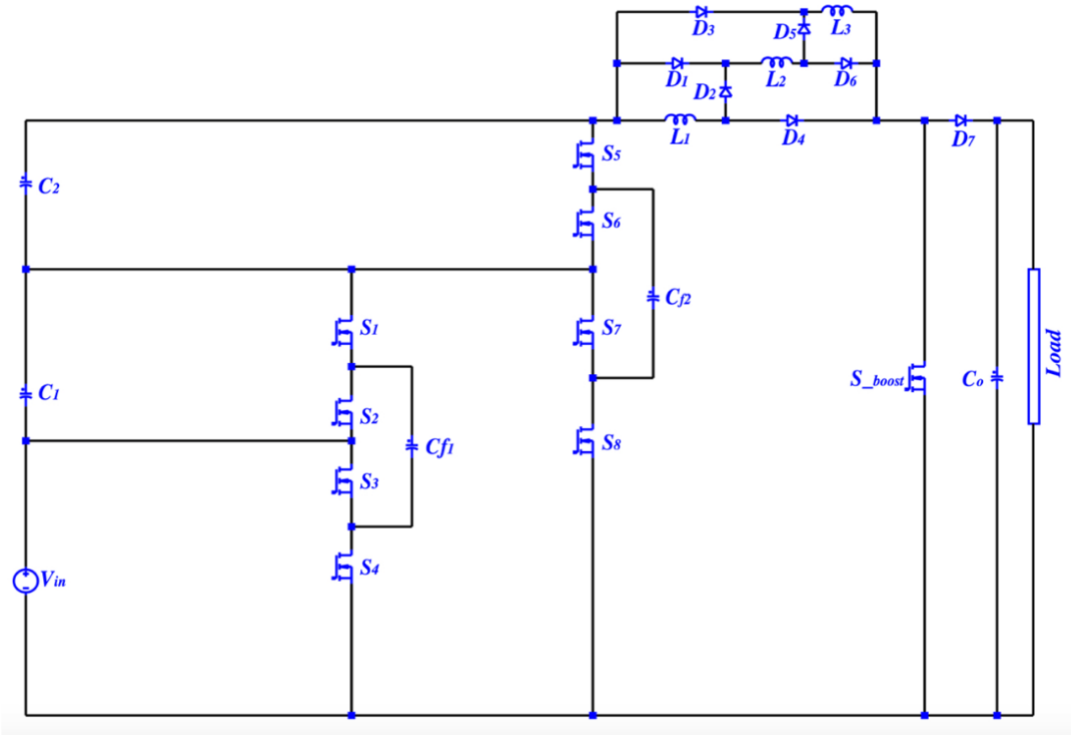
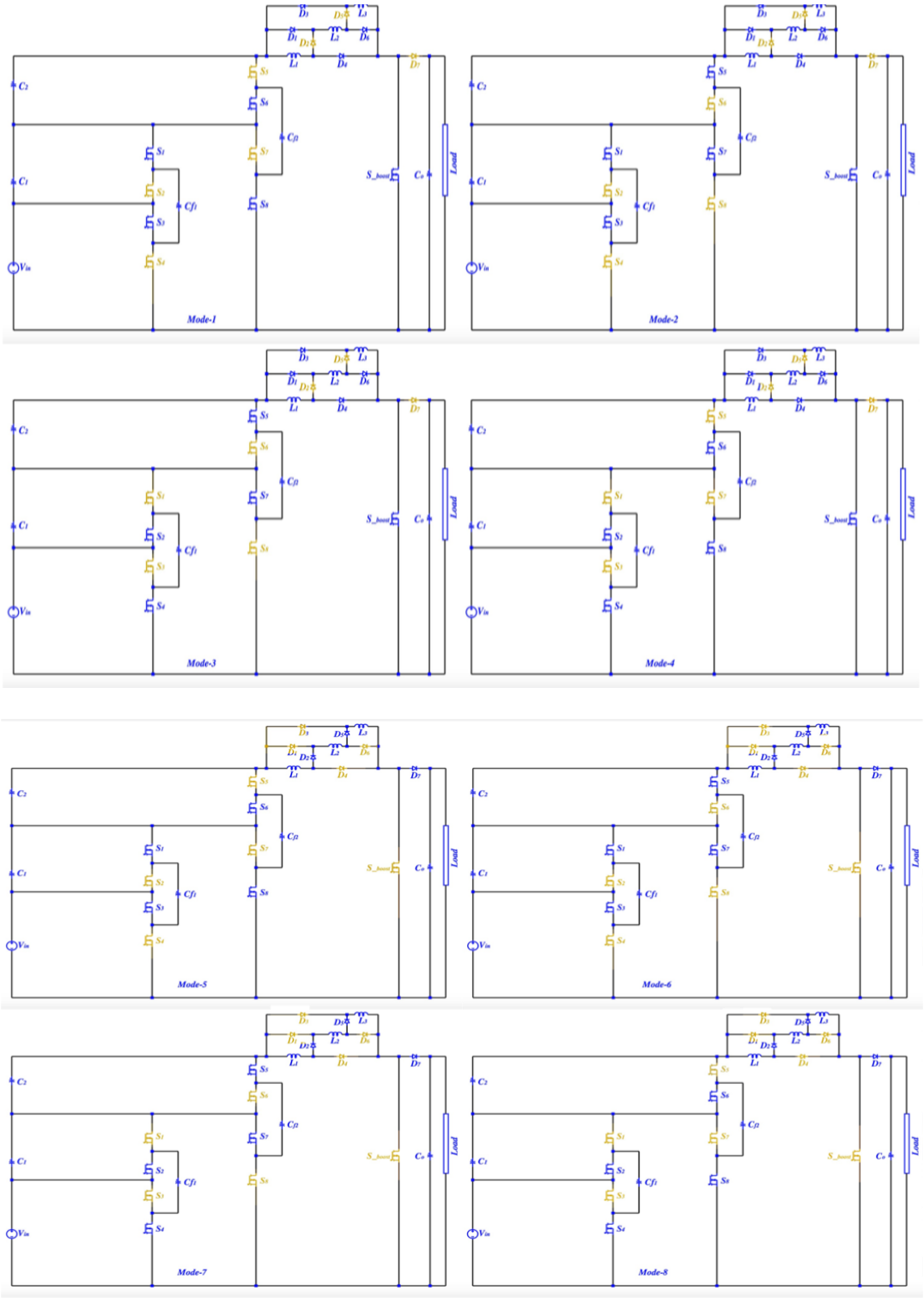


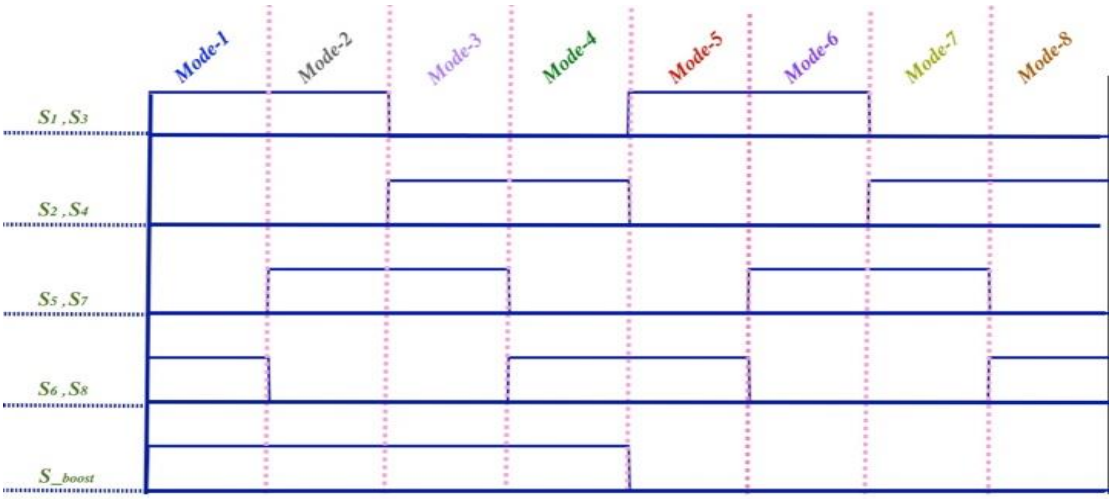
Figure 5.12: The 2 levels of the proposed PSC-boost converter proposed in [100].

5.8 Modes of operation of PSC-boost converter

Due to the control diagram in Figure 5.13-a, the switches S_1 to S_8 are controlled by a switching frequency that is double the switching frequency of $S_{\text{-boost}}$, which allows eight modes of operation to occur. The output voltage of the PSC converter has been regulated by switches' states that allow capacitors' charging and discharging. During Mode-1 to Mode-4, $S_{\text{-boost}}$ is on, then L_1, L_2, and L_3 are charged by the output of the PSC converter over D_1, D_3, D_4 and D_6 as in Figure 5.13-a. During Mode-5 to Mode-8, $S_{\text{-boost}}$ is off, and as a result D2, D5 and D7 are conducting, and then L_1, L_2, and L_3 have a series connection. Having a series connection of L_1, L_2, and L_3 allows the output capacitor to charge.



a) Operation modes



b) Control diagram

Figure 5.13: a) The operation modes of the PSC-boost converter. b) Timing diagram of the PSC-boost converter.

5.9 Analysis of the PSC-boost converter

As previously mentioned, a PSC converter output voltage is simply the input voltage of the switched-inductor boost converter. The three inductors L_1, L_2 and L_3 are assumed to be ideal and equal. Since L_1, L_2 and L_3 have a parallel connection during Mode-1 to Mode-4, they exhibit a voltage drop equal to V_{in} (5.14).

$$V_{in} = V_{L1} = V_{L2} = V_{L3} \tag{5.14}$$

$$I_c = \frac{-V_{out}}{R_L} \tag{5.15}$$

where V_{out} and R_L are the load voltage and resistor. During Mode-5 to Mode-8, S_boost is off, and L_1, L_2 and L_3 have a series connection.

$$V_{in} = V_{L1} + V_{L2} + V_{L3} + V_{out} \tag{5.16}$$

since L_1, L_2 and L_3 are identical, they will be charged equally.

$$V_{in} = V_{L1} + V_{L2} + V_{L3} + V_{out} \tag{5.17}$$

$$3V_L = V_{L1} + V_{L2} + V_{L3} \tag{5.18}$$

rewrite (5.17) into (5.18) to get (5.19)

$$V_{in} = 3V_L + V_{out} \tag{5.19}$$

$$V_L = \frac{V_{in} - V_{out}}{3} \tag{5.20}$$

When applying the inductor voltage's second balance to (5.14) and (5.20) to conclude voltage gain of the proposed model,

$$DV_{in} = -(1 - D)(\frac{V_{in} - V_{out}}{3}) \tag{5.21}$$

by simplifying (5.21), converter gain in the conventional form equals

$$\frac{V_{out}}{V_{in}} = \frac{2D+1}{1-D} \tag{5.22}$$

Since V_{in} of the input voltage of the switched-inductor boost converter is the output of the PSC converter, then

$$\frac{V_{out}}{V_{out\_PSC}} = \frac{2D+1}{1-D} \tag{5.23}$$

$$V_{out\_PSC} = 2^N V_{in} \tag{5.24}$$

where N is the number of the converter stages.

By rewriting (5.23), the voltage gain of the PSC-boost converter can be represented as

$$\frac{V_{out}}{V_{in}} = \frac{2^N(2D+1)}{1-D} \tag{5.25}$$

	PSC-boost (2-level)	**MBC (4-level)**
Number of S	5	1
Number of D	7	13
Number of C	5	7
Number of L	3	3
Voltage gain	$\frac{V_{out}}{V_{in}} = \frac{2^N(2D+1)}{1-D}$	$\frac{V_{out}}{V_{in}} = \frac{N(2D+1)}{1-D}$

Table 5.3: A comparison between the proposed PSC-boost and the MBC converter.

Parameter	**PSC-boost**	**MBC**
Input voltage	12	12
Switching frequency of *S*-*boost*	100 kHz	100 kHz
Switching frequency of S_1 to S_8	200 kHz	—
Diode type	MBRS240LT3	MBRS240LT3
Switches type	IRFI540NPbF	IRFI540NPbF
C_1 to C_7	94 uF	94 uF
C_{f1}, C_{f2} and C_o	198 uF	—

Table 5.4: Simulation parameters of the PSC-boost and the MBC converter.

5.10 Simulated results and a comparison of PSC-boost and MBC converter

The proposed converter's principles were studied by using the MATLAB SIMULINK and the LTspice software. Figure 5.14 shows converter's number of levels against the voltage gain of the PSC-boost converter and the MBC at a 50% duty cycle. Since the 2-level PSC-boost converter has a voltage gain equal to a 4-level MBC converter, a comparison between them is presented in this section. The two compared converters have same parameters as in Table 5.4. In the PSC-converter, two different switching frequencies, which are 200 kHz and 100 kHz, are chosen. The switches S_1 to S_8 operate at a 200 kHz switching frequency for a fixed duty cycle (50%) while 100 kHz is used for the $S_{\text{-boost}}$ switch. In the 4-level MBC converter, 100 kHz is used to operate the $S_{\text{-boost}}$.

One of the MBC converter's issues was that it could not regulate the actual voltage at a high duty cycle. Figure 5.15 represents a comparison between the 2-level PSC-boost and the 4-level MBC in the ability of achieving a voltage gain closer to the actual voltage gain as in (5.25). It can be seen clearly, the 2-level PSC-boost has a higher achieved voltage gain than the 4-level MBC at a higher duty cycle. The reason for that is replacing the uncontrollable switches of the MBC converter's voltage multipliers by fully controllable switches allows capacitors to charge and discharge comfortably. In addition to the voltage gain privilege, the 2-level PSC-boost converter has an output impedance less than the 4-level MBC converter Figure 5.17. Having a low output impedance means a high-power density and a small converter size. Furthermore, the 2-level PSC-boost converter has a higher efficiency than the 4-level MBC converter. Figure 5.16 shows a comparison between them in the fundamental efficiency at a varied rated power.

Table 5.5 contains prices of each elements used in this section. The proposed design (2-level of PSC-boost) converter as in Figure 5.12 has a number of elements where their total cost is $14.715. At the same regulated voltage gain, the 4-level MBC would cost $10.925. The cost increase is a tradeoff improving the rated output power, thus the PSC-boost converter's applications would be expanded. Furthermore, the PSC-boost converter shows a higher achieved efficiency where the highest efficiency was 93.7 % at 270W where 4-level of MBC only rated a 75W and achieved 89% efficiency. The 25% increase in the cost is a tradeoff increasing the efficiency by 5%.

Element	**Element Type**	**Price of each element**
Switch	IRFI540NPbF	$1.76
Diode	MBRS240LT3	$0.45
Capacitors	94 uF	$0.405
Inductance	1mH	$0.38

Table 5.5: Prices of each elements in Figure 5.11 and Figure 5.12 according to Digi-Key company.

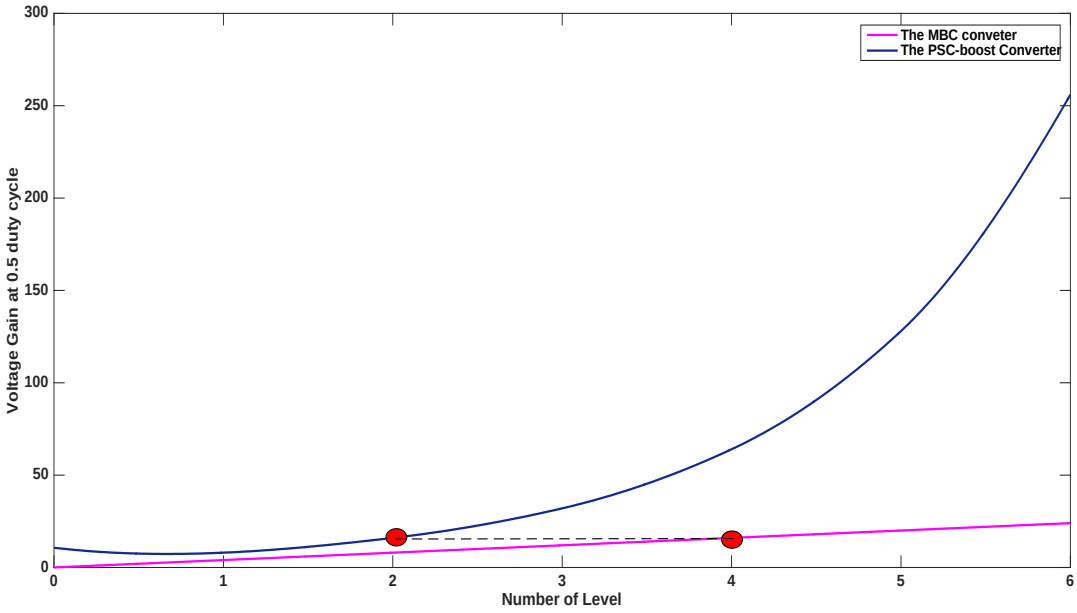


Figure 5.14: The number of levels against the voltage gain at 50% duty cycle of the MBC converter and the PSC-boost.

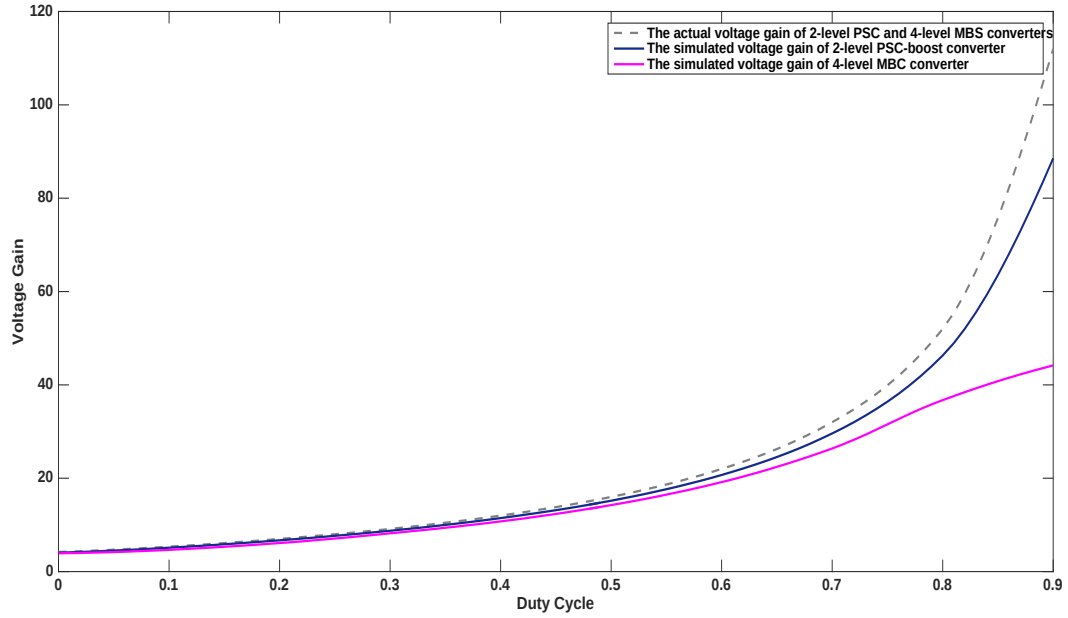


Figure 5.15: The duty cycle against the voltage gain of the 4-level MBC converter and the 2-level PSC-boost.

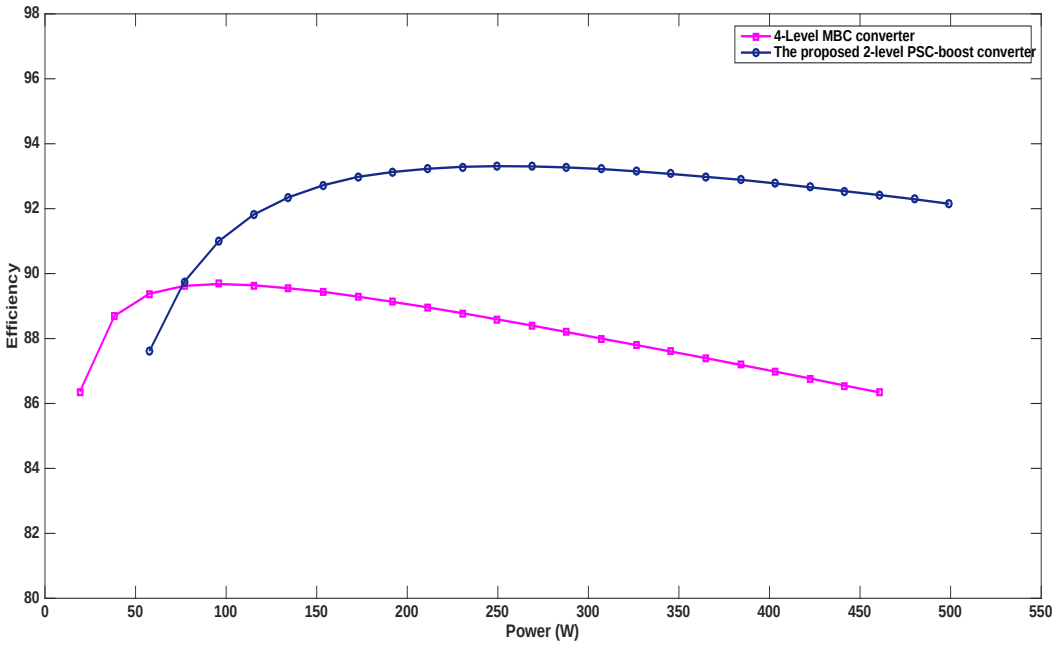


Figure 5.16: The overall efficiency of the 2-level PSC boost and the 4-level-MBC.

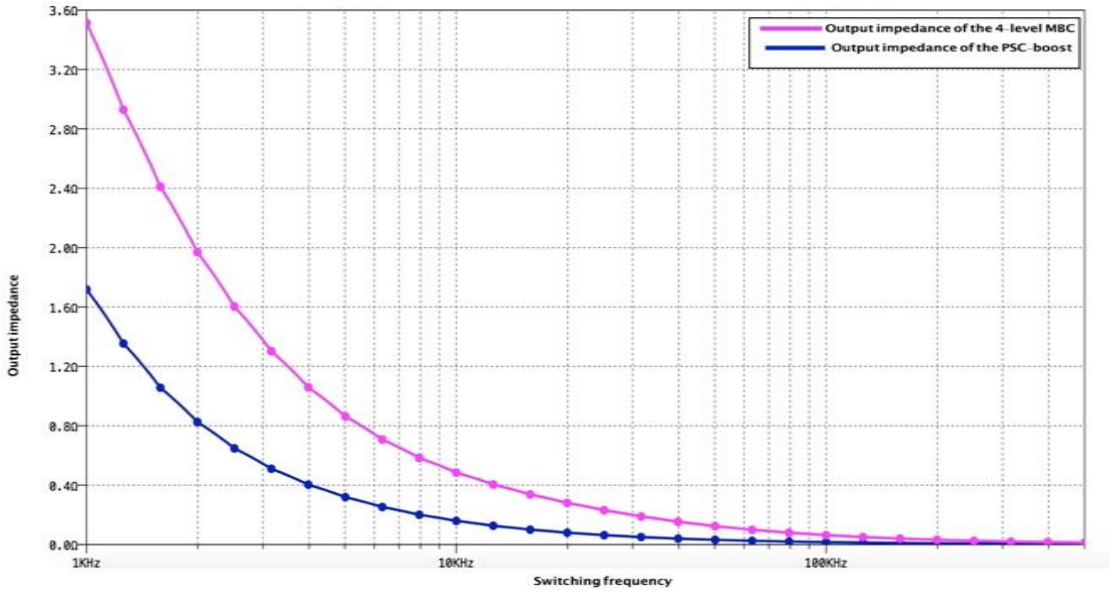


Figure 5.17: The output impedance of the 2-level PSC boost and the 4-level-MBC at a different switching frequency.

CHAPTER SIX: CONCLUSION AND FUTURE WORK

6.1 Conclusion

The SC converters have promised to be an alternative converter for the traditional DC-to-DC converters. The reason why SC converters are more preferable for small circuit integrations is that SC converters have a high-power density due to the absence of magnetic elements. However, designing a SC topology must meet some requirements such as a smaller number of elements and high efficiency. In addition to that, reducing the output impedance is another challenge for designing SC converters. In this work, a SC converter topology has been proposed with a smaller number of elements and a lower output impedance. The proposed PSC converter has shown higher efficiency achievement due to lower output impedance over other topologies.

The proposed split-phase control allows the 1-to-4 PSC converter to operate in the complete soft-charging operation. The elimination of the current transient excellently increases both the efficiency and the power density. In addition to the output impedance reduction, the complete soft-charging operation leads to eliminating the voltage mismatch between any parallel capacitors. The complete soft-charging achievement helps to reduce the switching frequency requirement, which is essential for output impedance reduction. A theoretical analysis was successfully applied for resizing the capacitors in the soft-charging approach. Beyond the resizing approach, the theoretical analysis productively helps to calculate the duty cycles for each operation mode. The dead time of the proposed control

diagram is the main reason behind achieving superior efficiency due to smaller switching losses and lower output impedance. However, a lower capacitor size causes a higher output voltage ripple. An output LC filter was added to the 1-to-4 PSC converter to reduce the output voltage ripple. Adding the LC filter could cause a small loss; however, this loss is not effective to the efficiency which has been efficaciously increased by using the complete soft-charging-II technique.

SC converters are usually used as voltage multiplier cells which are connected to the traditional non-isolated converter to improve the voltage gain. One of the best known SC converters to be used as voltage cells is the multilevel voltage cell. These multilevel cells are usually connected to the output side of the DC-to-DC boost converter without altering its primary side. This work also has implemented the MBC by proposing a switched-inductor model to be used instead of the single inductor in the design. Since MBC has a single switch which is a pivotal component, the proposed switched-inductor design successfully helps reduce the switch voltage stress. In addition to the stress reduction, the proposed switched inductor MBC has shown an improvement in voltage gain which leads to increase $I_{\mathrm{out,DEF}}$ and rated output power. The simulated and theoretical results have shown some discrepancies which are related to the parasitic components of inductors, capacitors, and semiconductor elements. Two chosen models of switched inductor design as in [2][3] and [4][5] were compared with the proposed model. The three level MBC was supplied by 12 V at 50 kHz $\boldsymbol{f_{sw}}$ with a 75% duty cycle. In the proposed design, both V_{DEF} and I_{DEF} have successfully reached double increases as compared to [2][3], but with an appropriate 35% increment over a MBC in [4][5]. Since both V_{DEF} and I_{DEF} have increased,

then the output power of MBC will be increased as well. On the other hand, adding more components to the MBC is one of the proposed design drawbacks which could affect the efficiency.

The switched-capacitors insertion into a boost converter was successfully completed in this work. Cascading a switched-capacitor converter to a traditional boost converter results in a new boost converter that works similarly to the MBC converter. A comparison between the 4-level MBC converter and 2-level PSC-boost converter was simulated by using a MATLAB/SIMULINK and LTspice. The proposed converter has a privilege over the MBC in the high voltage gain achievement at a higher duty cycle assumption. Due to uncontrollable switches (diodes) and the short switch's time off, the output capacitors in the MBC converter fail to charge and discharge completely. The proposed converter contains a switched inductor model [14] participating as the inductor of the conventional boost converter. In addition to the higher voltage gain achievement, the PSC-boost converter has a higher achieved fundamental efficiency. Since the PSC- boost has a smaller number of components, it has a higher power density than the MBC converter.

6.2 Future Work

- As mentioned in section 3 and 4, the purpose behind using the soft-charging operation instead of soft-switching operation to improve the converter performance is because the soft-charging operation does not require any additional components. However, since both soft-switching and soft-charging techniques help to increase the efficiency and implement the output impedance, in this work applying the soft-charging to the PSC has only used and proven where the soft-switching technique needs to be investigated and

compared with it. The suggested future work based on using the soft-switching operation should be aware of the resonant element sizes in order to maintain the power density.

- Investigation of the stability of the proposed PSC may be accomplished by studying the small signal analysis. In addition to that, a feedback control diagram is suggested to be designed for the two-stage PSC converter or for a higher order of the proposed converter.
- The analysis and discussion of the proposed PSC was based on disregarding the parasitic components of the capacitors. The consideration of the parasitic components of the capacitors needs to be investigated and compared with experimental work. In addition to that, a small signal analysis after considering the parasitic components of the capacitors is recommended.
- In section 5.6 regarding applications, the proposed converter can be used for a renewable energy application such as in a PV system. The appropriateness of using the proposed converter in the renewable energy system needs to be investigated further.

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Appendix

List of Publications

Journal

1. **A. Alateeq**, Y. Almalaq, and M. Matin, "A Performance of the Soft-Charging Operation in Series of Step-Up Power Switched-Capacitor Converters," *Journal of Low Power Electronics and Applications*, vol. 8, no. 1, p. 8, Mar. 2018.

2. **A. Alateeq**, and M. Matin, "Soft-Charging Effects on High Gain DC-to-DC Step-up Converter with PSC Voltage Multipliers.," *Journal of Low Power Electronics and Applications* (submitted).

Conference

3. **A. Alateeq**, Y. Almalaq, and M. Matin, "A switched-inductor model for a non-isolated multilevel boost converter," in *2017 North American Power Symposium, NAPS 2017*, 2017, pp. 1–5.

4. **A. S. Alateeq**, Y. A. Almalaq, and M. A. Matin, "Modeling a multilevel boost converter using SiC components for PV application," Proc. SPIE 9957, Wide Bandgap Power Devices and Applications, 99570J (19 September 2016)

5. **A. Alateeq**, Y. Almalaq, and M. Matin, "Using SiC MOSFET in Swictched-Capacitor Converter for High Voltage Applications," in *2016 North American Power Symposium, NAPS 2016*, 2016, no. 2, pp. 16–20.

6. **A. Alateeq** and M. Matin, "A Novel Design of a High Gain Step-up Converter Using Switched-Capacitors/Switched-Inductors Cells," in *2018 IEEE International Conference on Electro Information Technology (EIT)*, 2018, pp. 102–106.

7. Y. Almalaq, **A. Alateeq**, and M. Matin, "Non-isolated high gain switched inductor DC-DC multilevel cuk converter for photovoltaic applications," in *2017 North American Power Symposium (NAPS)*, 2017, pp. 1–5.

8. Y. Almalaq, **A. Alateeq**, and M. Matin, "A Transformerless High Gain Switched-Inductor Switched-Capacitor Cuk Converter in Step-Up Mode," in *2018 IEEE*

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9. Y. Almalaq, **A. Alateeq**, and M. Matin, "Simulation and performance comparison of Si and SiC-based interleaved boost converter," Proc. SPIE 10381, Wide Bandgap Power Devices and Applications II, 103810C (23 August 2017).

10. Y. Almalaq, **A. Alateeq**, M. Matin, "Silicon carbide DC-DC multilevel Cuk converter," Proc. SPIE 9957, Wide Bandgap Power Devices and Applications, 99570I (19 September 2016).

11. Y. Almalaq, **A. Alateeq**, and M. Matin, "Three Topologies of a Non-Isolated High Gain Switched-Inductor Switched-Capacitor Step-Up Cuk Converter for Renewable Energy Applications," in *2018 IEEE International Conference on Electro Information Technology (EIT)*, 2018, vol. 7, no. 6, p. 94.

12. **A. S. Alateeq**, Y. A. Almalaq, M. Matin, "Modeling and simulation of GaN step-up power switched capacitor converter," Proc. SPIE 10381, Wide Bandgap Power Devices and Applications II, 103810G (23 August 2017).